

CONTENT	SHEET
Cover Sheet, Block diagram	1-2
Intel LGA775 CPU - Signals/ Power/ GND	3-5
Intel Eaglelake - FSB, PCIE, DMI	6
Intel Eaglelake - VGA, MSIC	7
Intel Eaglelake - Memory DDR2	8
Intel Eaglelake - Power / GND	9-10
ICH10DO - PCI, USB, DMI, PCIE	11
ICH10DO - Host, DMI, SATA, Audio, SPI, RTC, MSIC	12
ICH10DO - Power, GND	13
DDR2 Chanel-A / Chanel-B	14-15
Clock Gen - ICS9LPRS113	16
Super I/O Fintek F71882	17
VGA	18
SATA / e-SATA / FAN Control	19
LAN Intel82567 (OPT1-vPro)	20
JMB-368 IDEX1 (PCIE)	21
JMB-381 1394 (PCIE)	22
Audio Codec ALC888	23
PCIE x16, x1	24
DVI transfer & switch	25
DISPLAY PORT	26
PCI Slot 1 & 2	27-28
Rear/Fount USB Connector	29
System Power/ACPI Controller UPI	30
DDR2 / NB-Core Switching Power	31
VRD11 - ISL6334 4Phase	32
ATX Power-Con. / F_Panel	33
Manual & Option Parts	34
Revision History	35

MS-7562 UATX Version: 1.1

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Yorkfield processors in LGA775 Package.

System Chipset:

Intel Eaglelake - Q45 (North Bridge)
Intel ICH10DO (South Bridge)

On Board Device:

CLOCK Gen -- ICS9LPRS113A
LPC Super I/O -- Fintek F71882F
LAN -- LAN Intel 82567
JMB368 IDEX1
JMB381-1394
HD Audio Codec -- ALC888
PCIE to DVI Interface
PCIE to Display port Interface


Main Memory:

Dual-channel DDR-II * 4

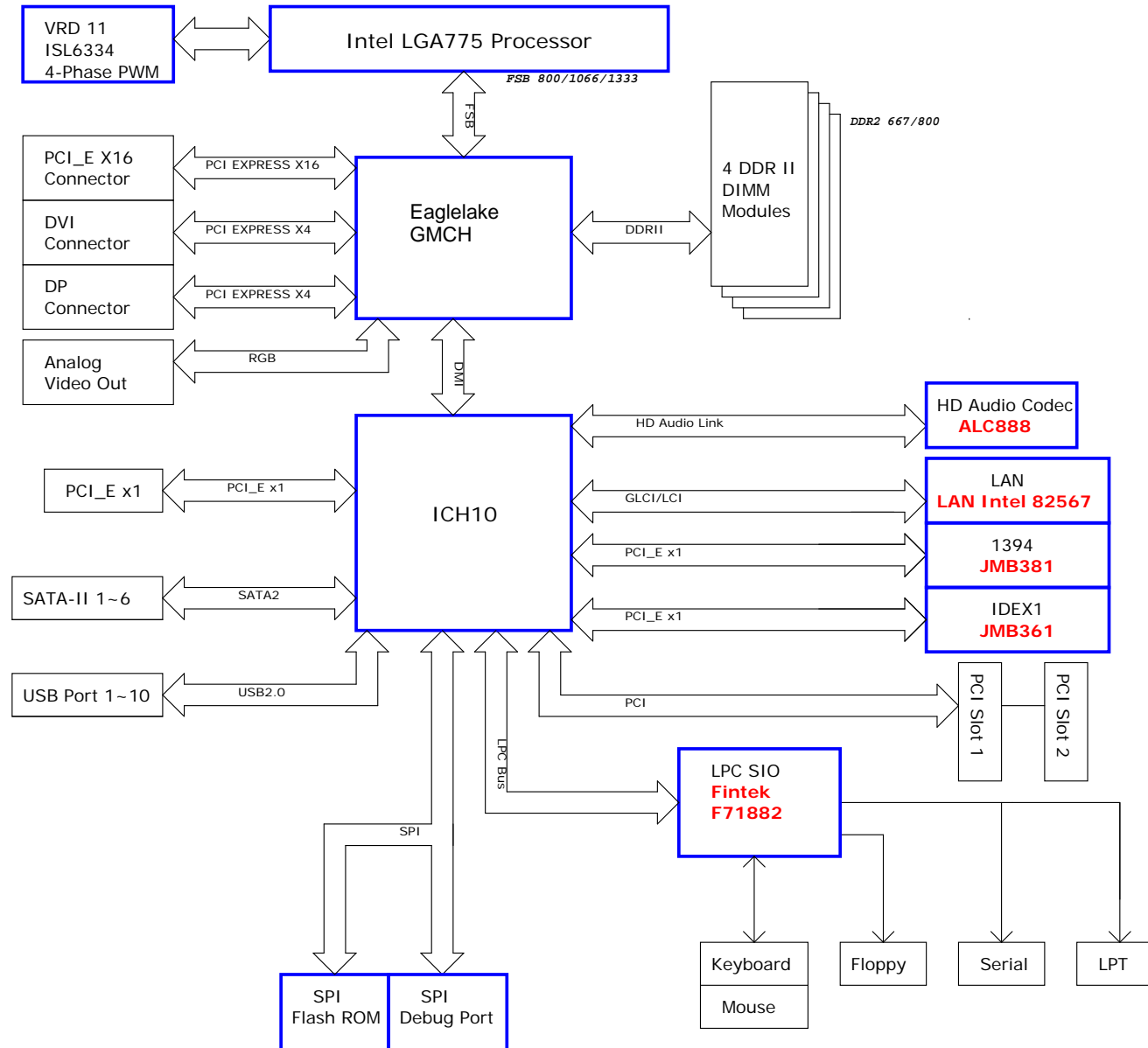
Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X4 share to DVI
PCI EXPRESS X4 share to Display port
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 2

PWM: ISL6334 4Phase

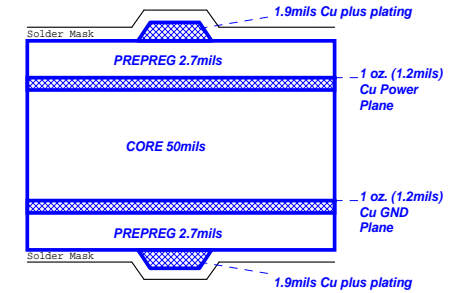
				MICRO-STAR INT'L CO.,LTD			
				MS-7562			
Size	Custom	Document Description	COVER SHEET	Rev	1.1		
Date:	Wednesday, December 03, 2008	Sheet	1	of	39		

Block Diagram



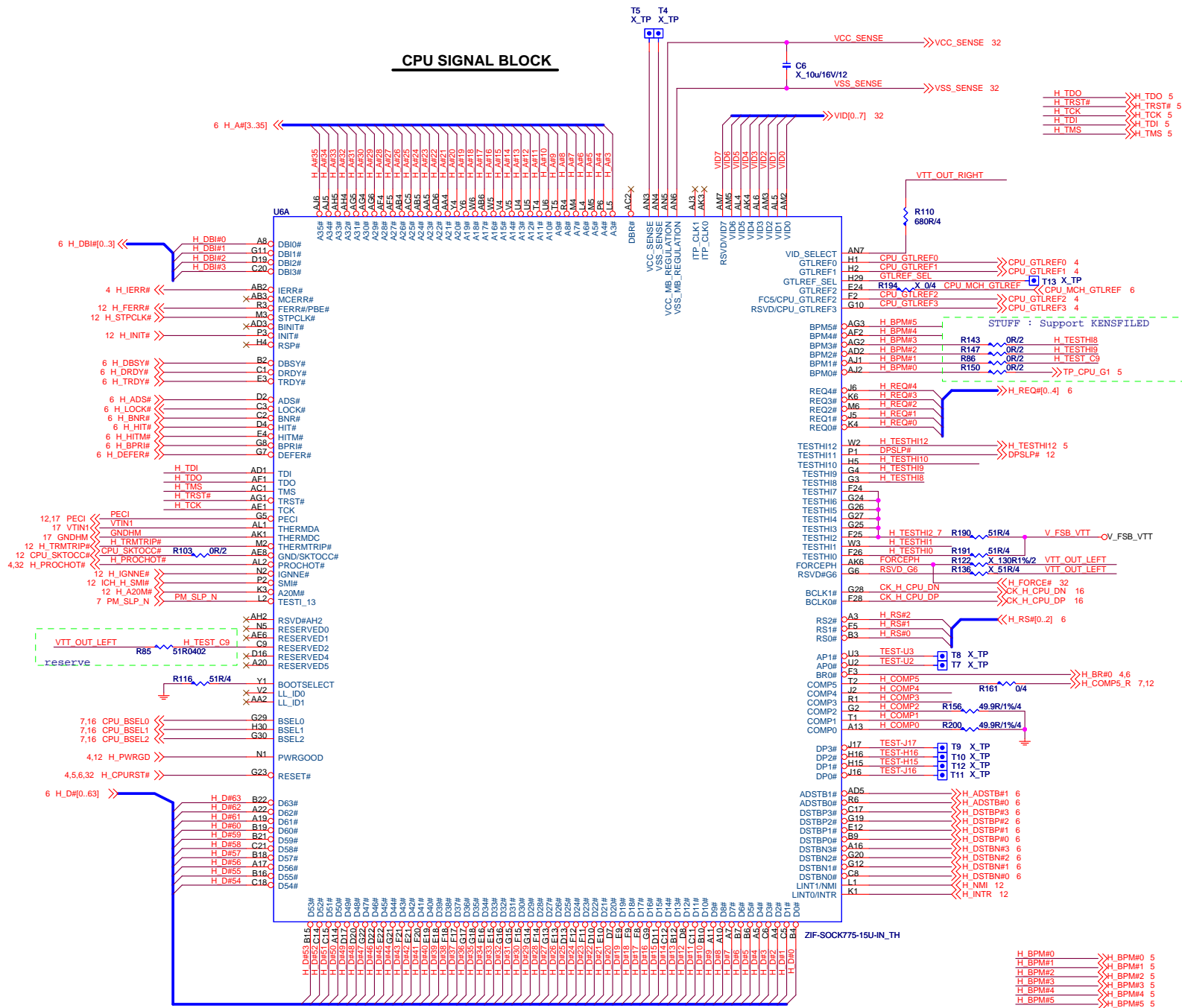
Board Stack-up

(1080 Prepreg Considerations)

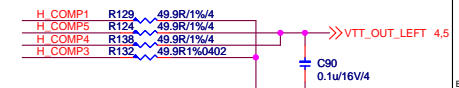
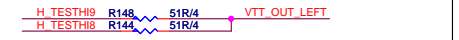
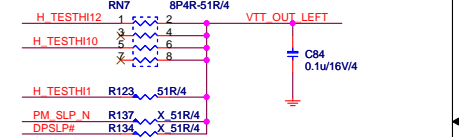
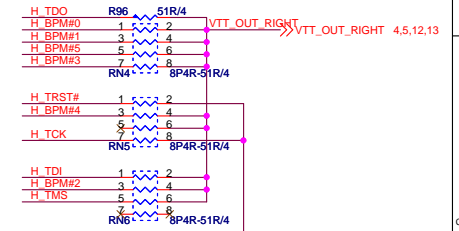
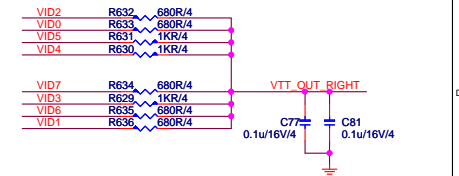


Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15

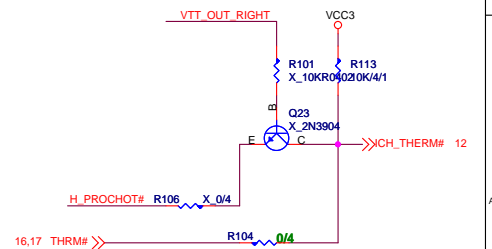
CPU SIGNAL BLOCK



PULL HIGHT PULL DOWN



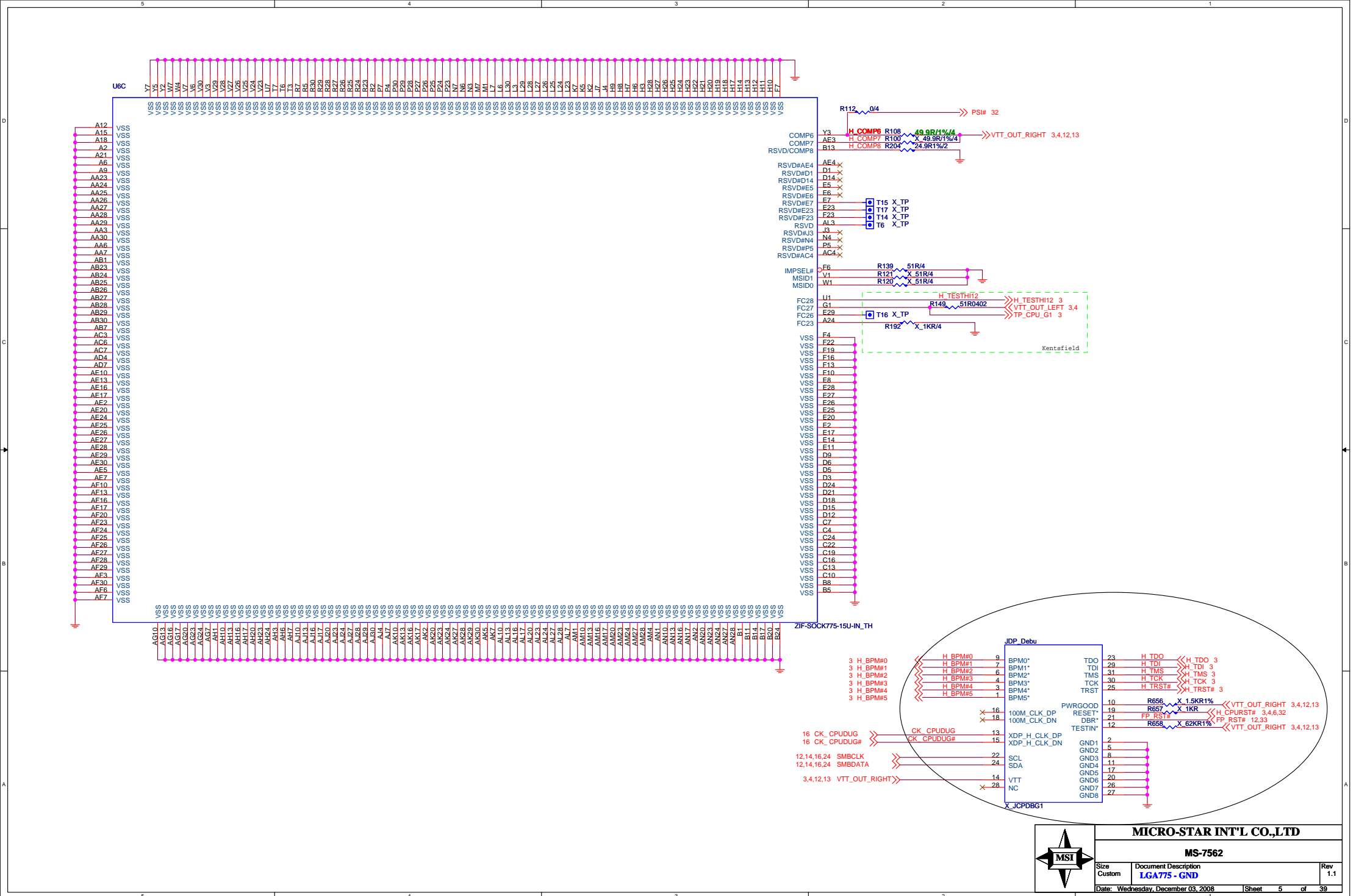
Thermal TRIP




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MS-7562

Size Custom	Document Description LGA775 - Signal	Rev 1.1
Date: Friday, December 05, 2008		Sheet 3 of 39

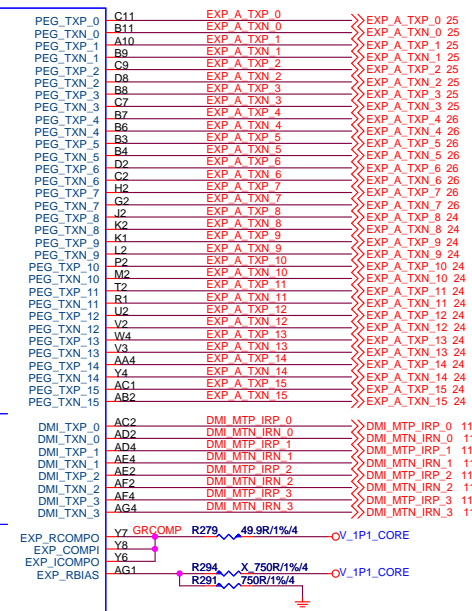
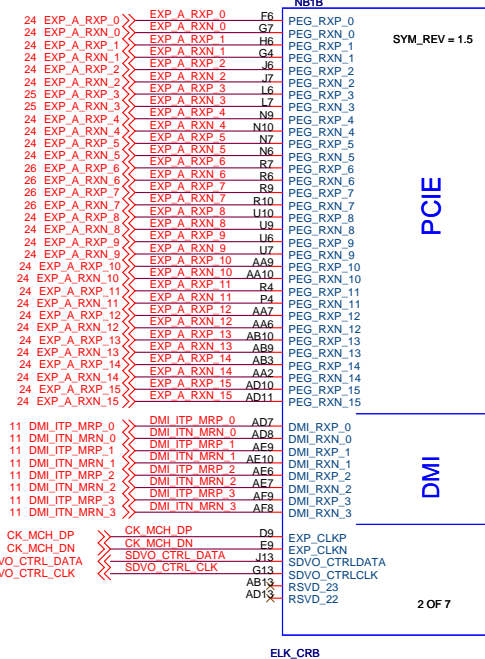
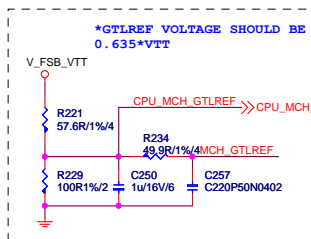
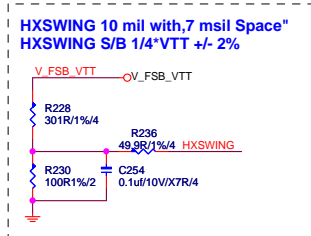
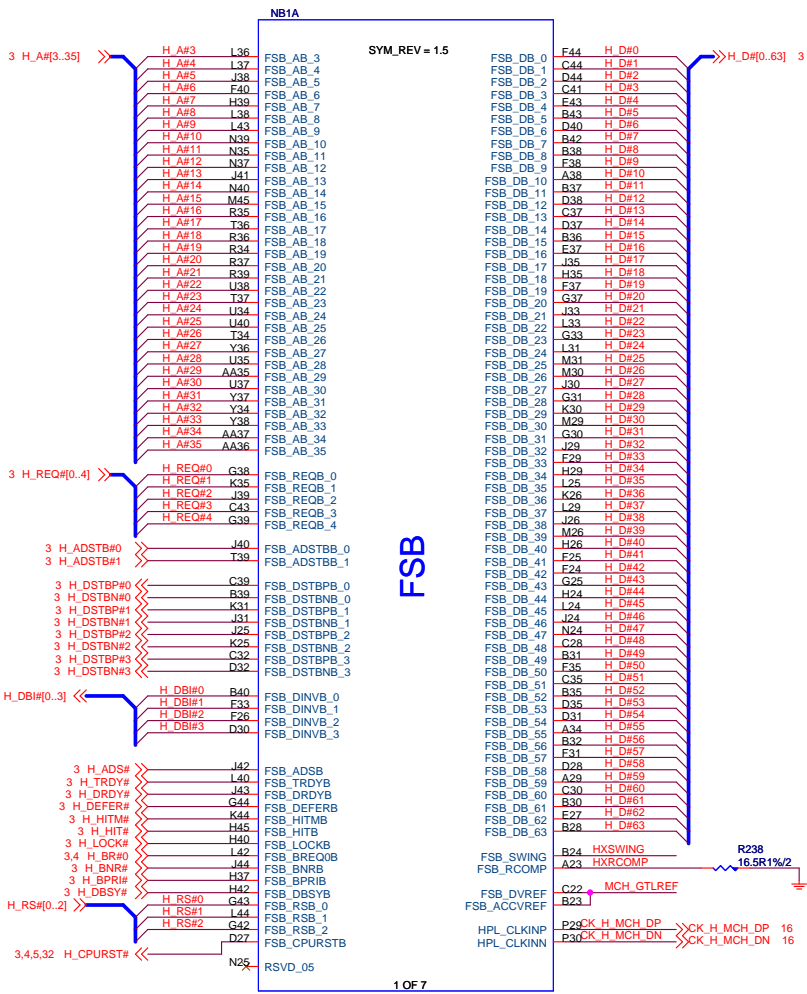


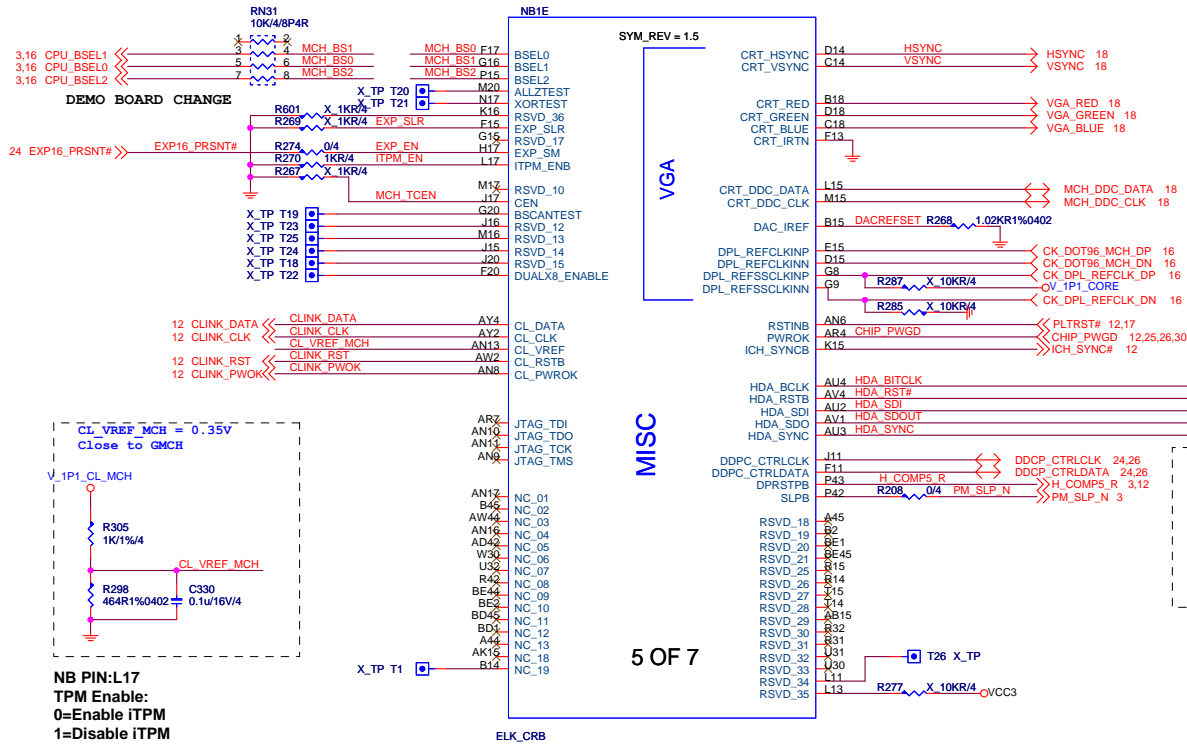


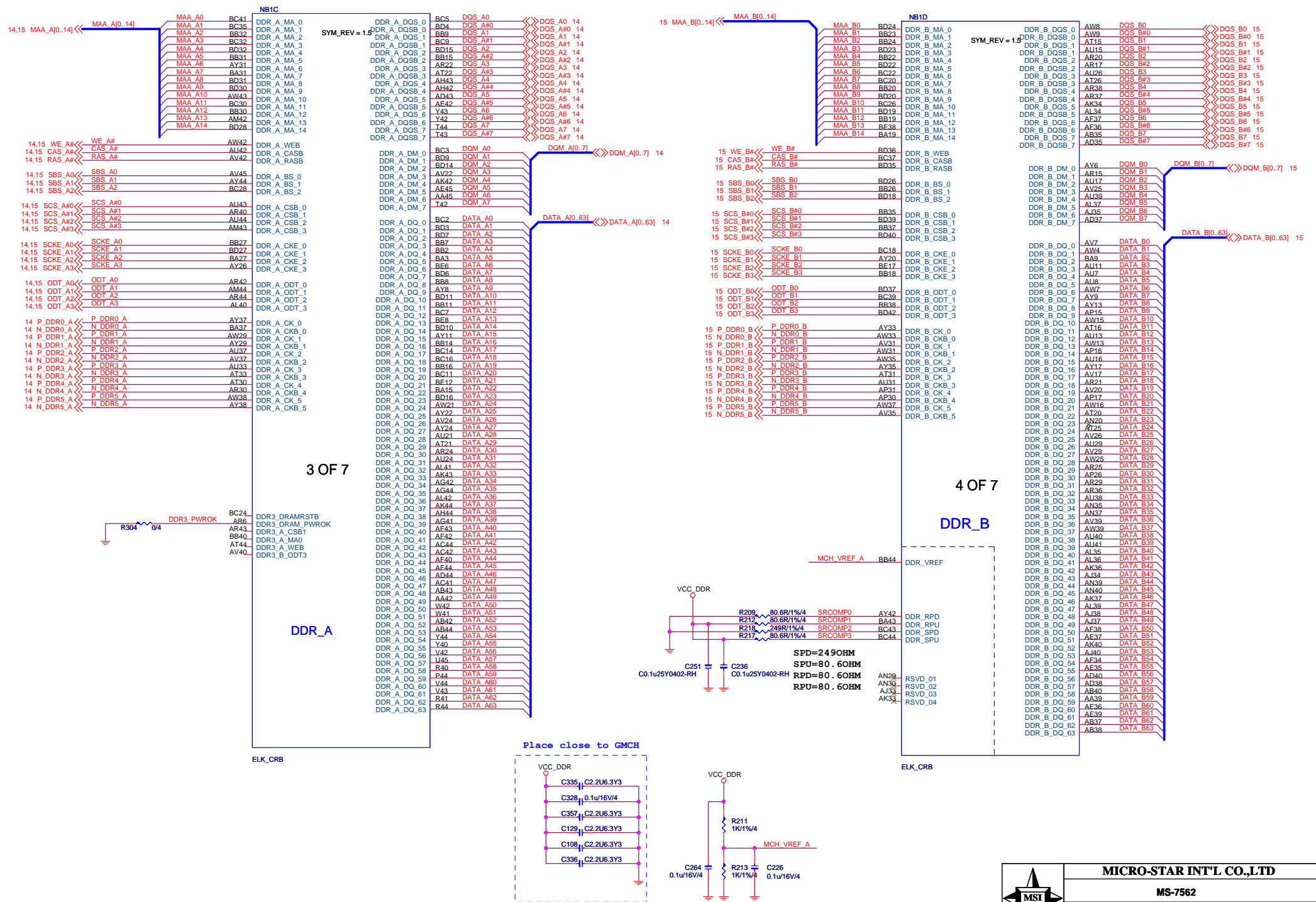
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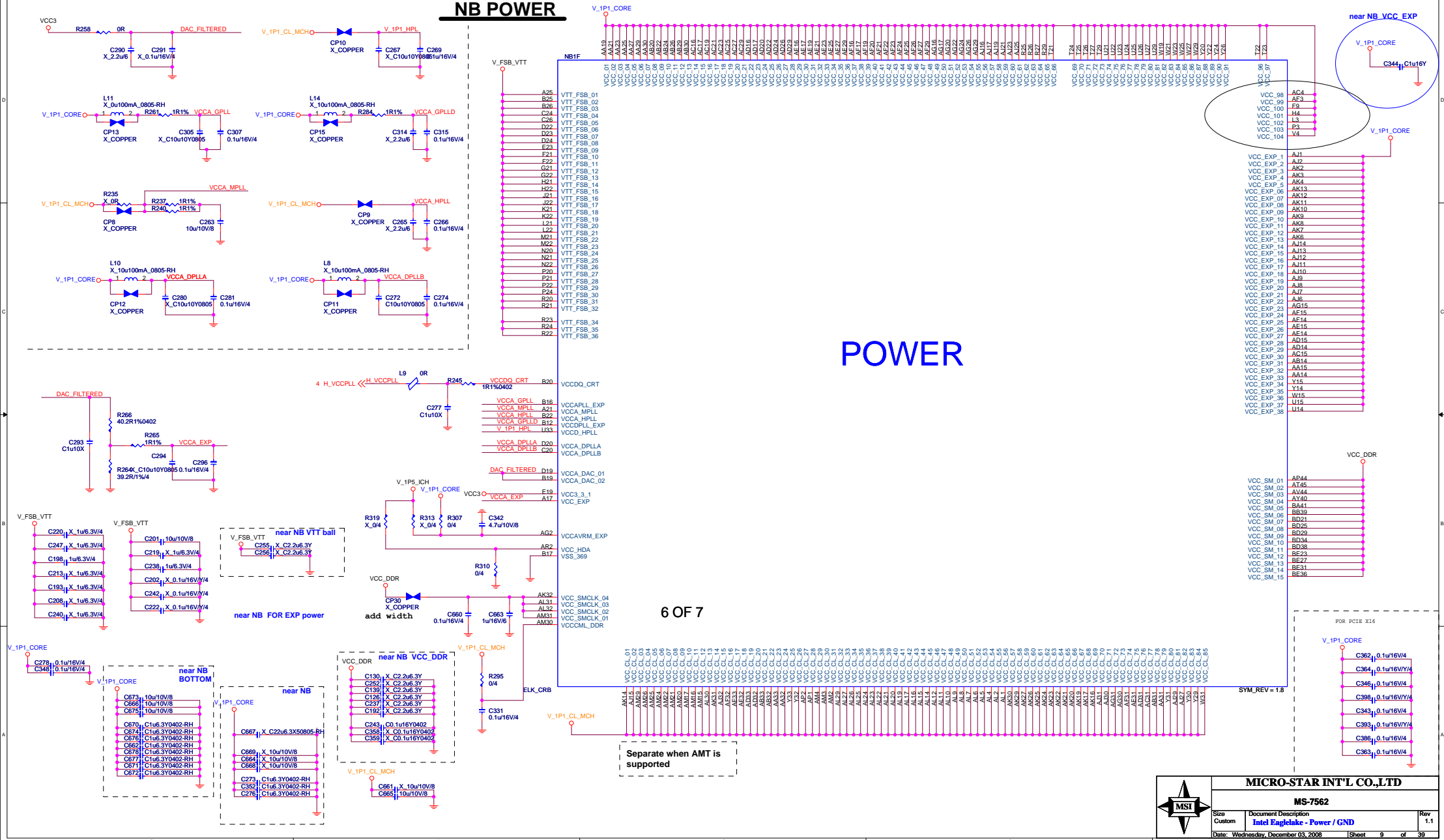
Size	Document Description	Rev
Custom	LGA775 - GND	1.1
Date: Wednesday, December 03, 2008		Sheet 5 of 39







NB POWER



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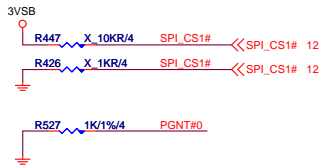
MS-7562

Size Custom	Document Description Intel Eaglelake - Power / GND	Rev 1.1
Date: Wednesday, December 03, 2008		Sheet 9 of 39

GND

70F 7

SB STRAPPING RESISTOR



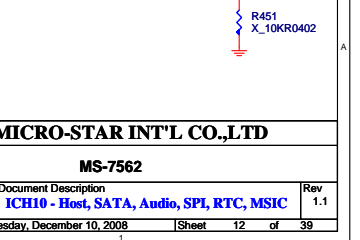
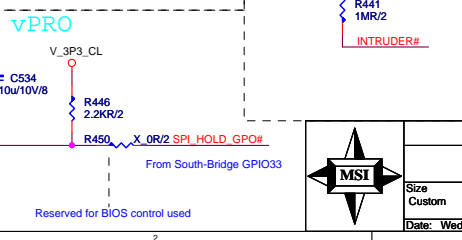
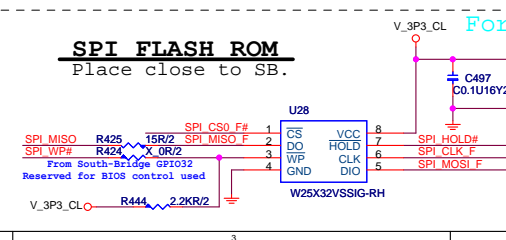
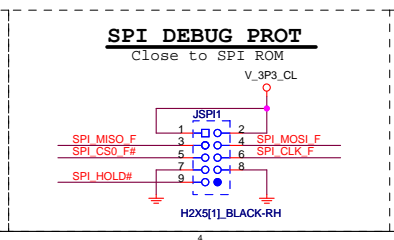
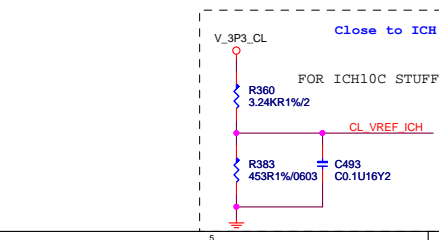
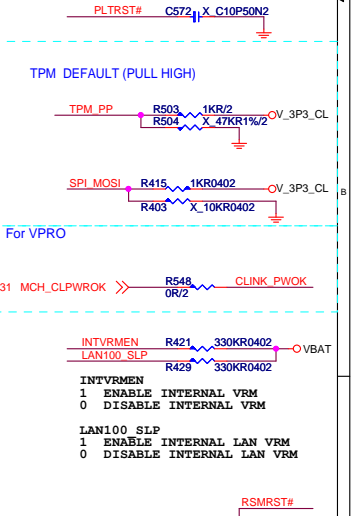
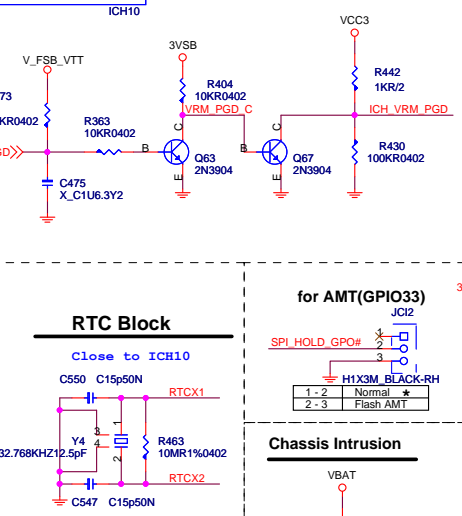
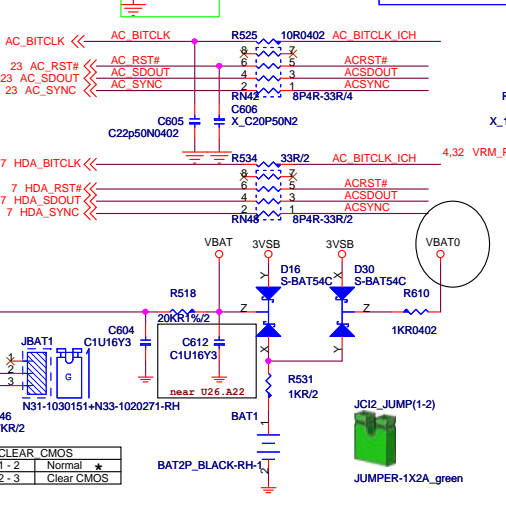
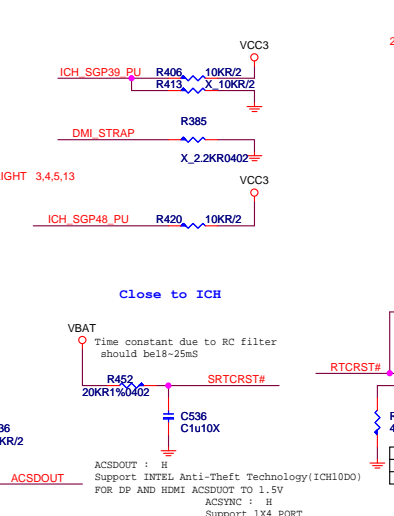
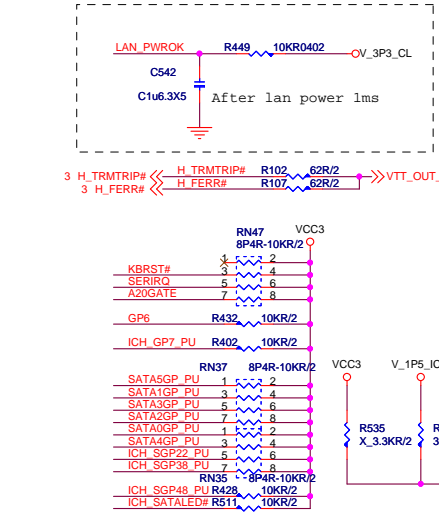
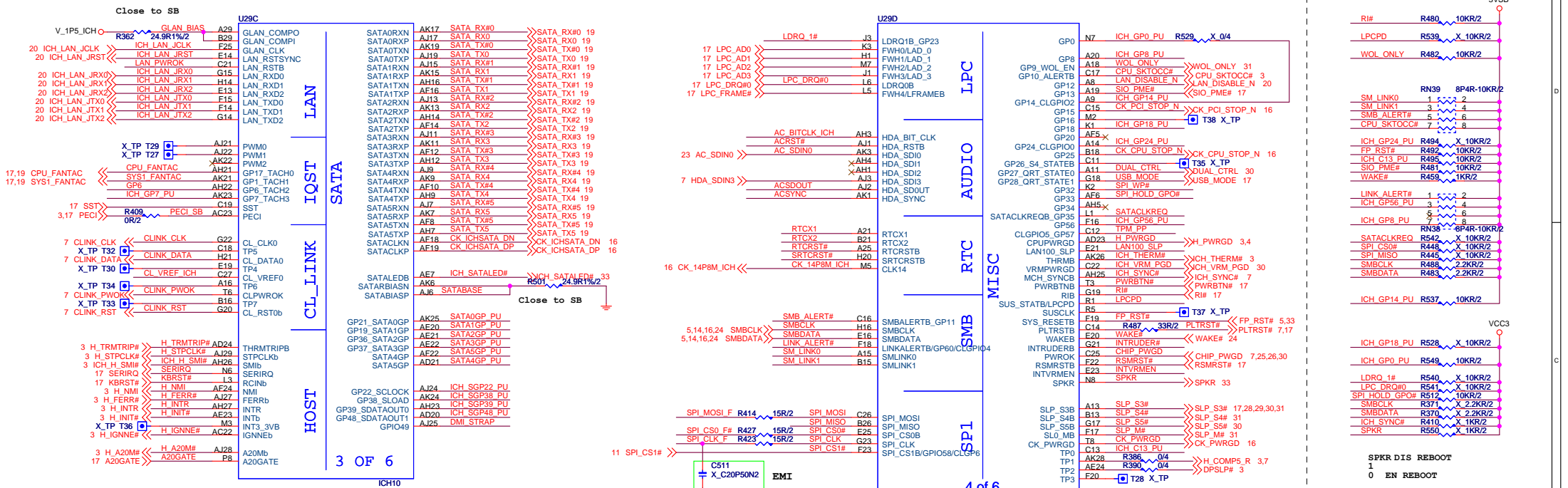
PGNT#[3:0] Internal Pull-up

SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

HDA_SDOUT/HDA_SYNC strap PCI_E port configuration bit[1:0]. Internal weak pull down.
00:1X/1X/1X/1X 11:0X/0X/4X

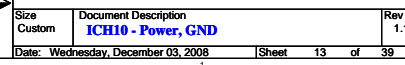
BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	X
PCI	1	0

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MS-7562			
Size Custom	Document Description ICH10 - PCI, DMI, USB, PCIE & Slots		Rev 1.1
Date: Wednesday, December 03, 2008		Sheet 11	of 39

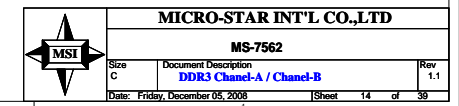


V5REF must be powered up before VCC3 or after VCC3 within 0.7V. Also, V5REF must power down after VCC3 or before VCC3 within 0.7V. This rule is also applies to V5REF_SUS and 3VSB. However, the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore, they can satisfy the requirement.

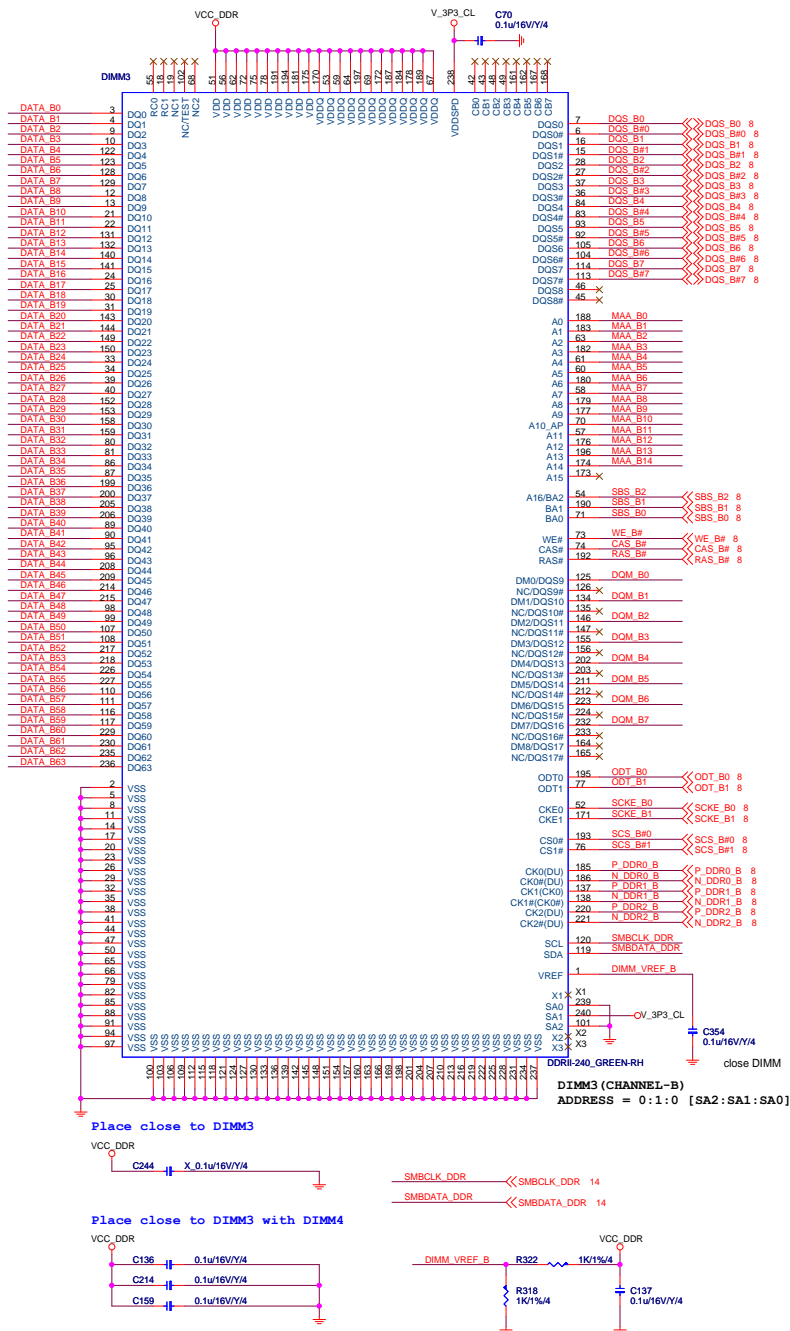


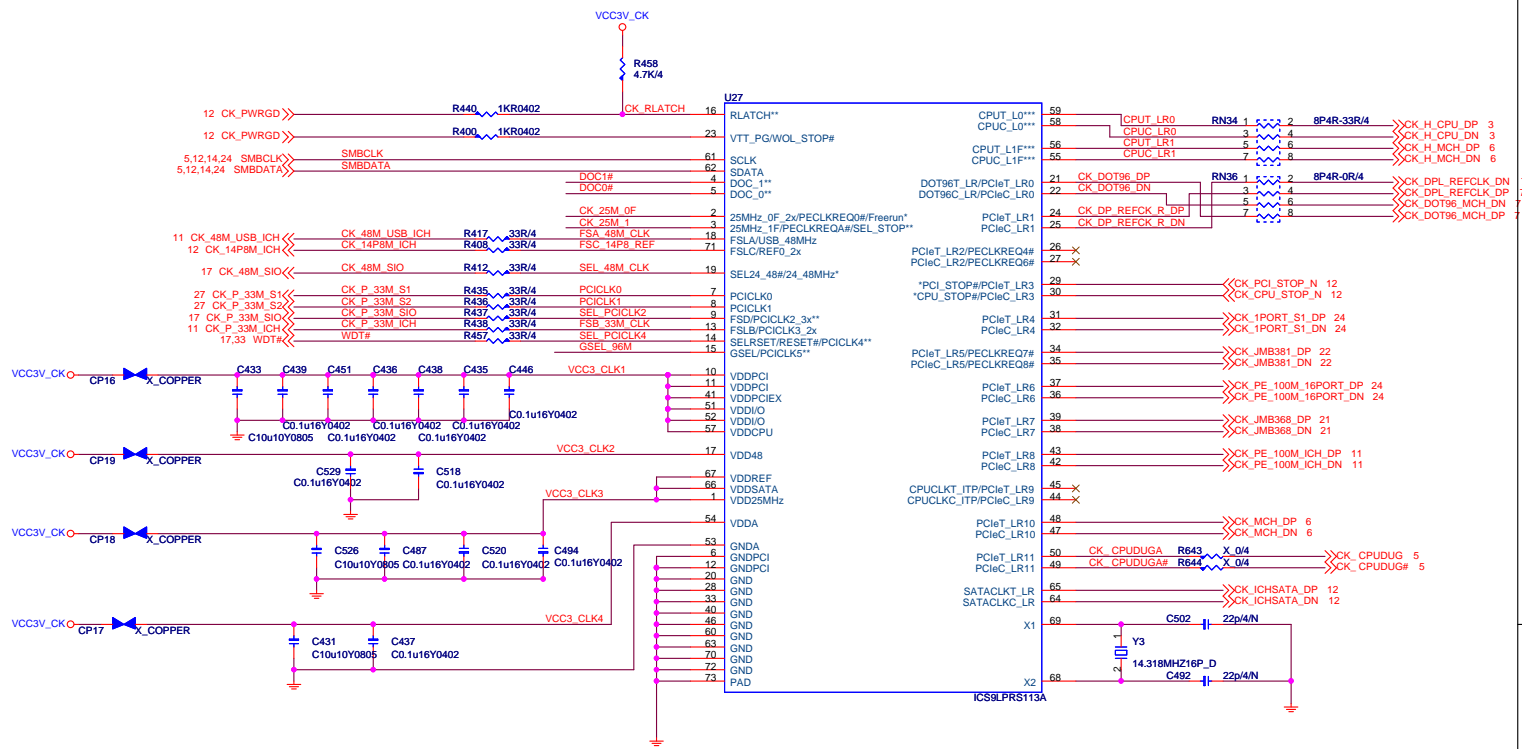


DDRII DIMM_A2

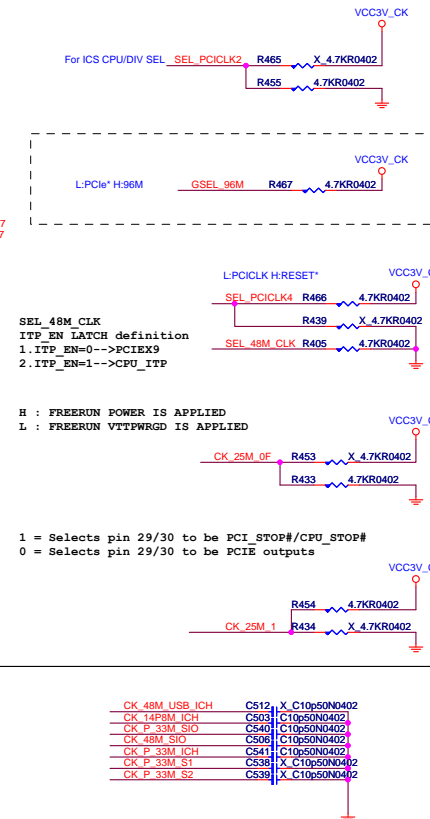


DDR2 DIMM_B1

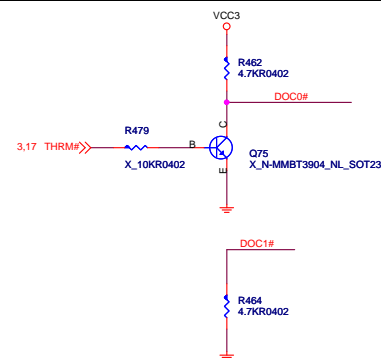
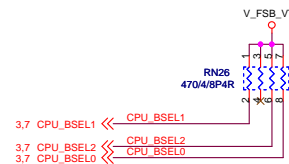




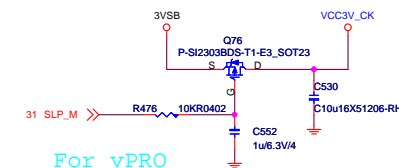
CLOCK GEN STRAPING



BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHz (1066)
1	0	0	333 MHz (1333)
0	1	0	200 MHz (800)
1	1	0	400 MHz (1600)



AMT POWER

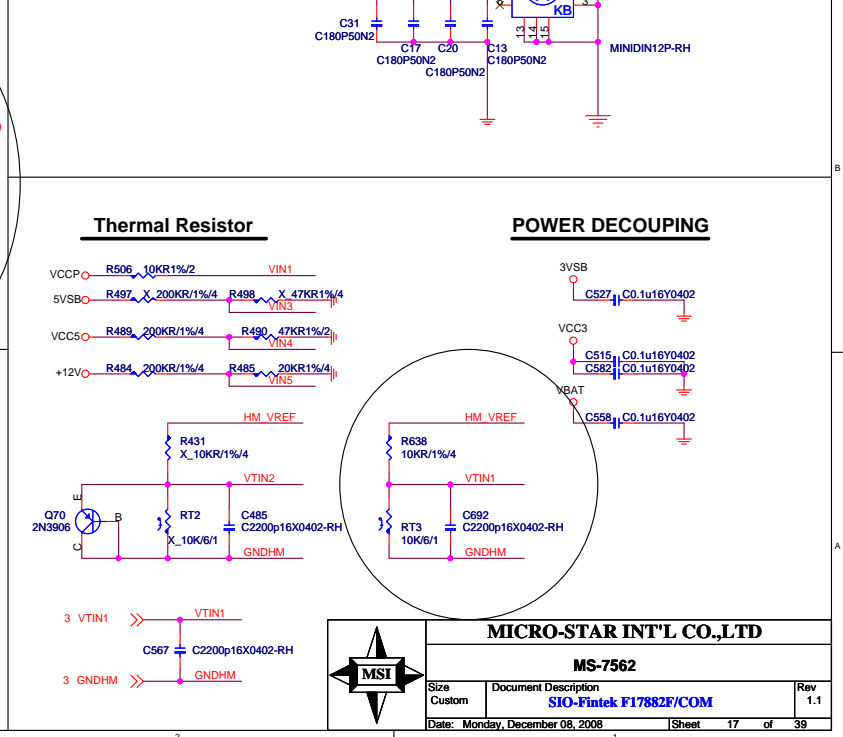
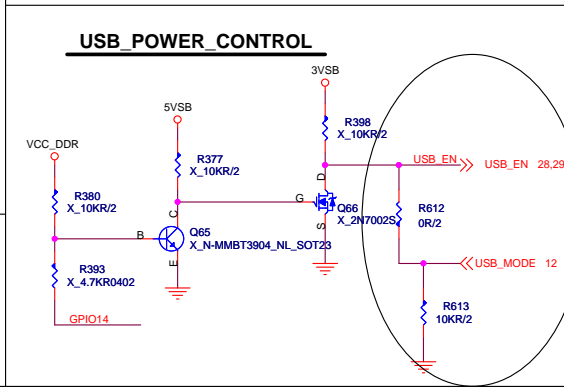
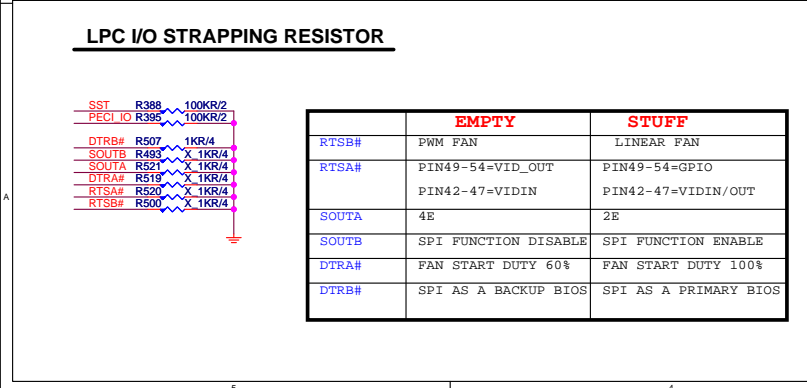


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MS-7562

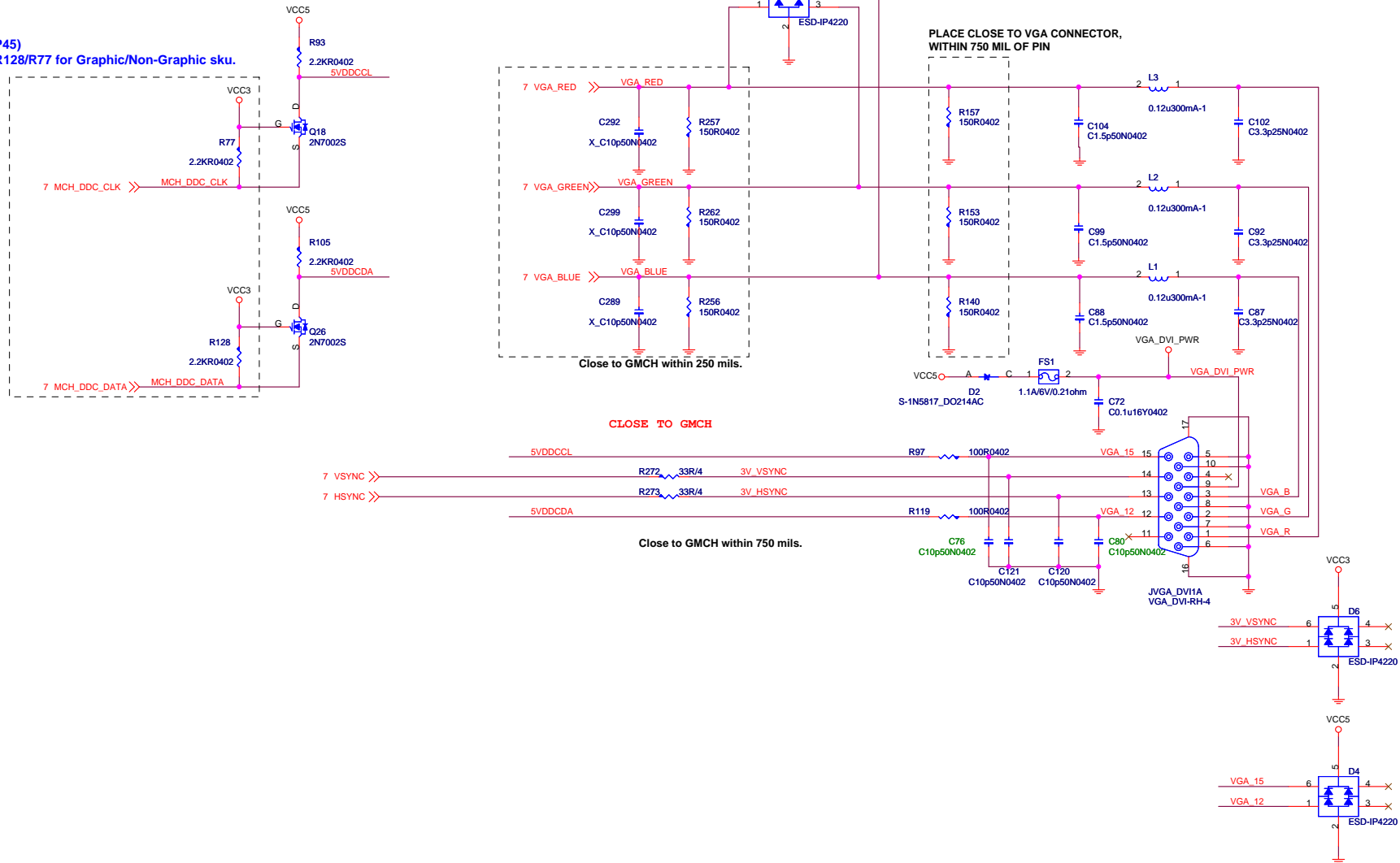
Size Custom	Document Description Clock Gen ICS9LPRS113
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Rev	1.1
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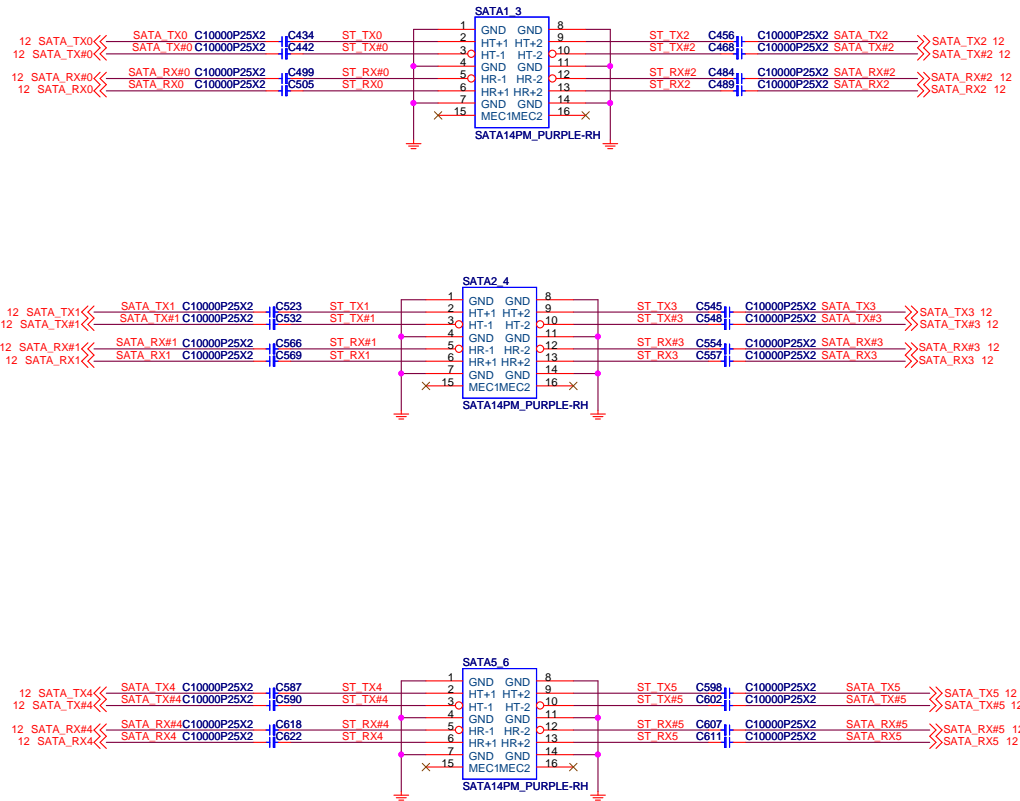


Video Connector

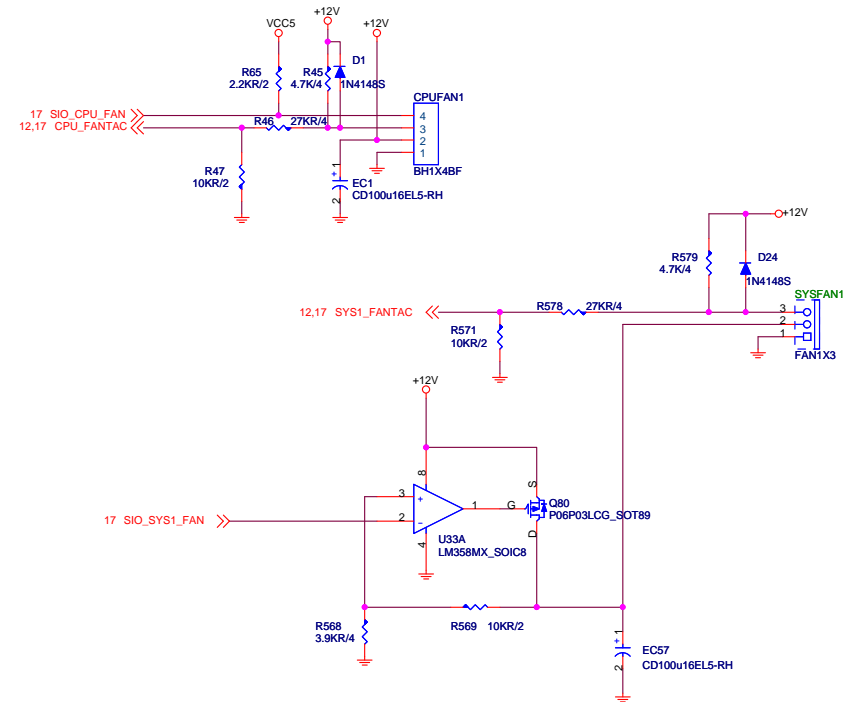
FOR V10 (NB:P45)
Always Stuff R128/R77 for Graphic/Non-Graphic sku.




SATA 1- 6 PORT



FAN-COUNTDOWN CIRCUIT



			
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MS-7562			
Size	Document Description	Rev	
Custom	SATA & e-SATA Ports and Fan Control	1.1	
Date: Wednesday, December 03, 2008		Sheet	19 of 39

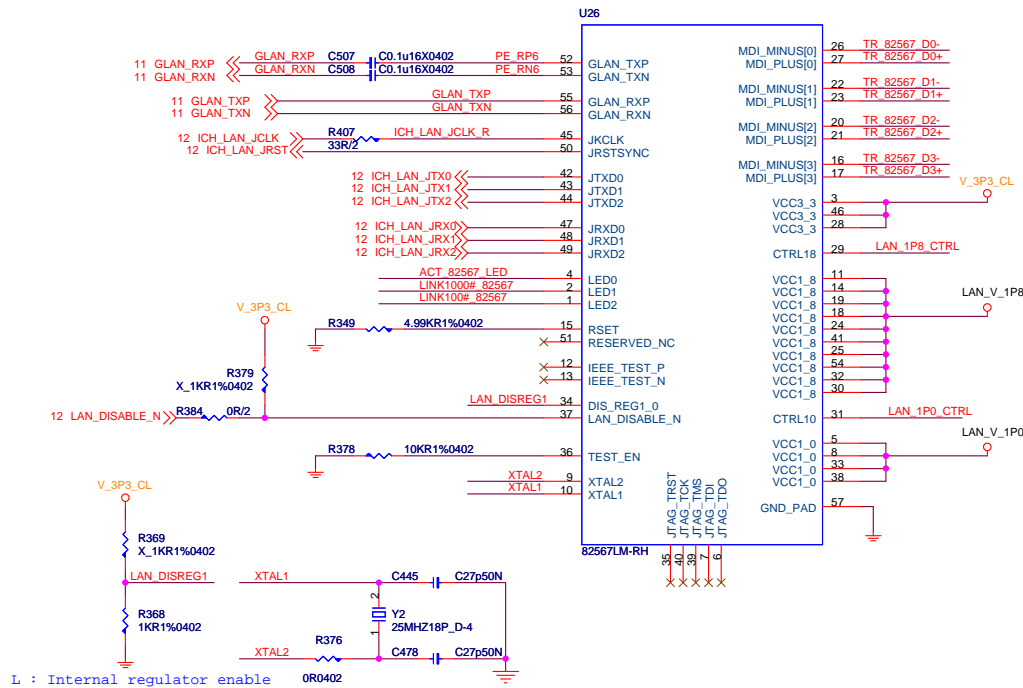
Maximum current of 1.8 V is less then 270mA, Maximum current of 1.0 V is less then 139mA.

For proper and safe operation, the power supplies must follow the following rule:

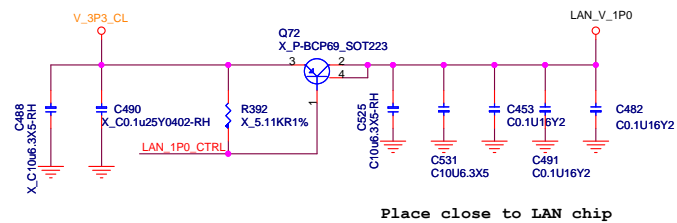
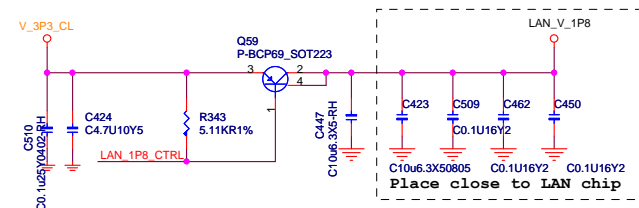
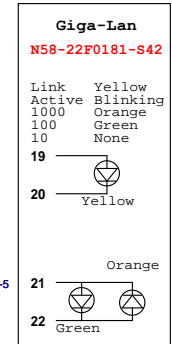
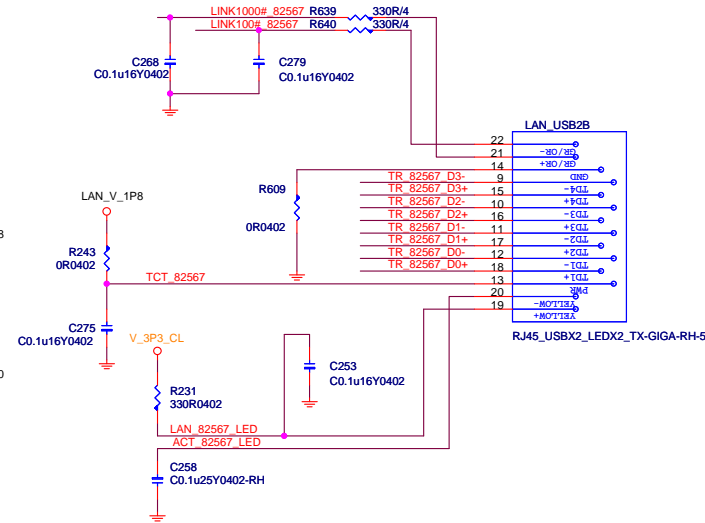
VDDO (3.3V) \geq AVDD (1.8) \geq DVDD (1.05V)

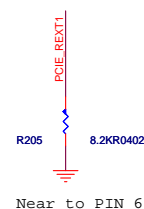
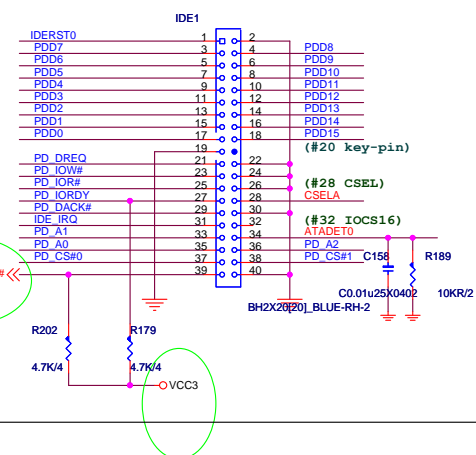
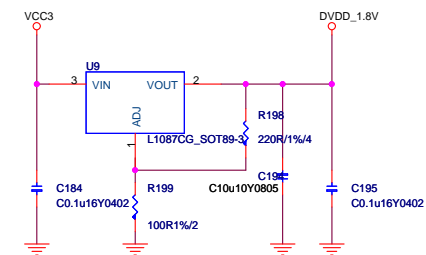
This means that VDDO must start ramping before AVDD and DVDD, but DVDD may reach its nominal operating range before AVDD and VDDO.

FOR V10 (NB:P45)
LAN_USB1B ==> N53-08M0171-K06



EMI Solution





1394 CONTROLLER

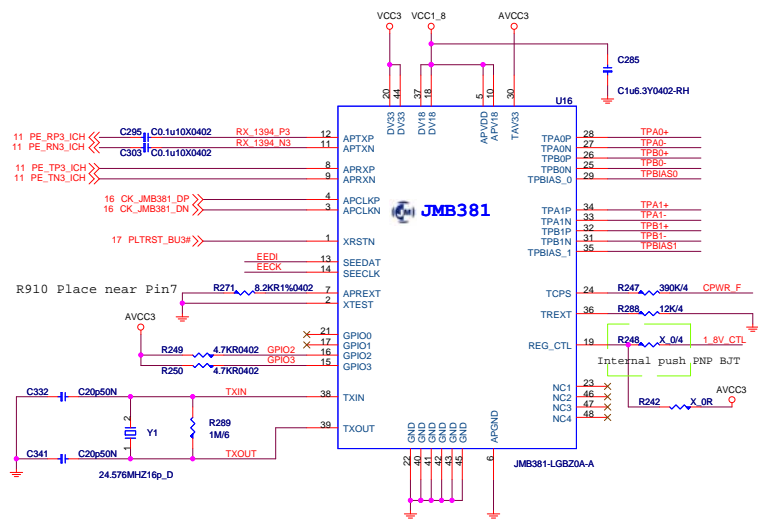
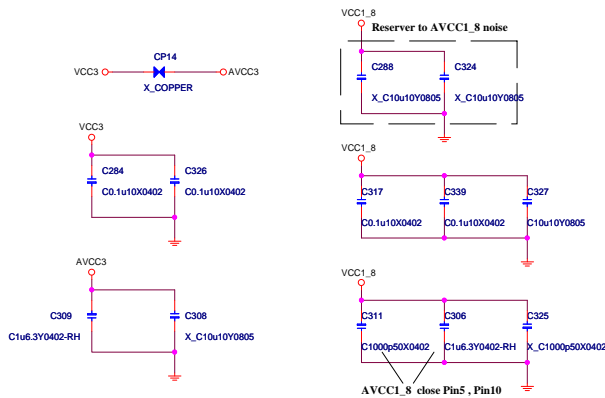
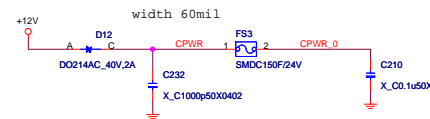
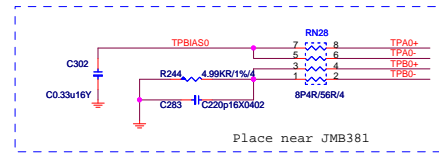
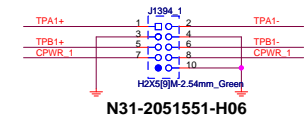
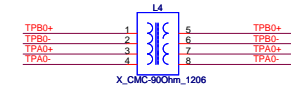
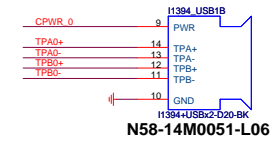
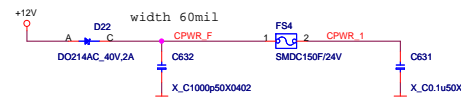
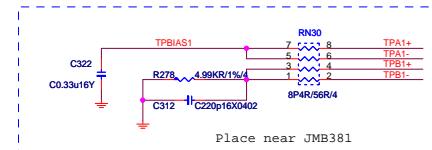


Table 5.1 JMB381 Operating Modes

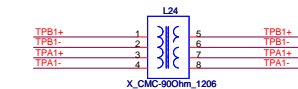
	Normal	IDDQ	BIST/FL	Nandtree
XTEST	0	1	1	1
GPIO2	x	0	0	1
GPIO3	x	0	1	1

Rear 1394 port

Front 1394 pin header

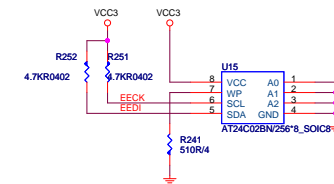
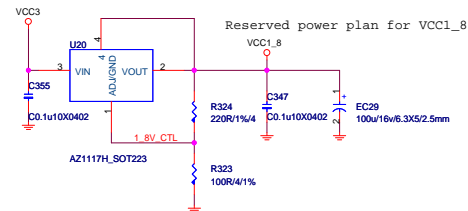


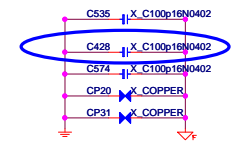
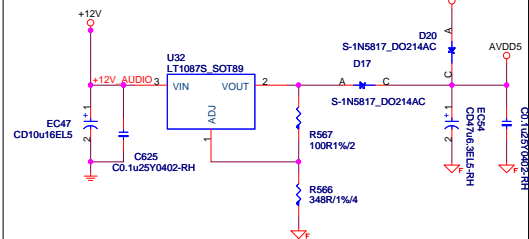
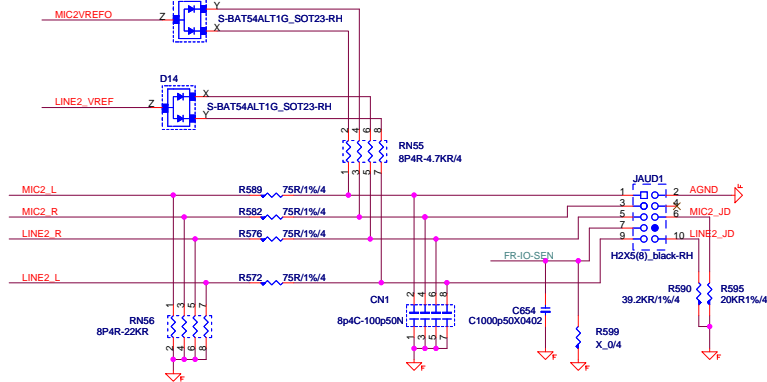
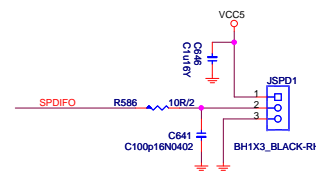
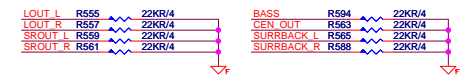
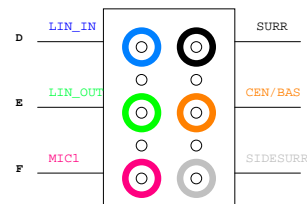
For Intel 1394 pinheader



EMI request 11/28

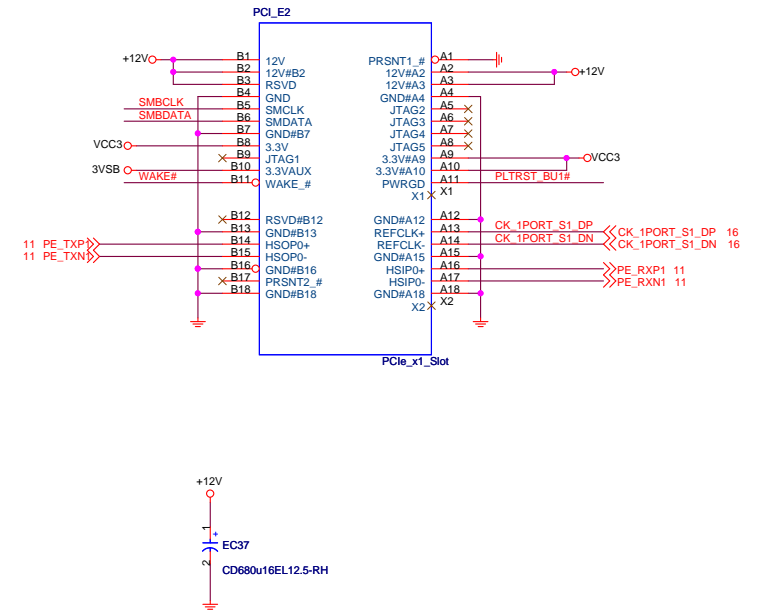
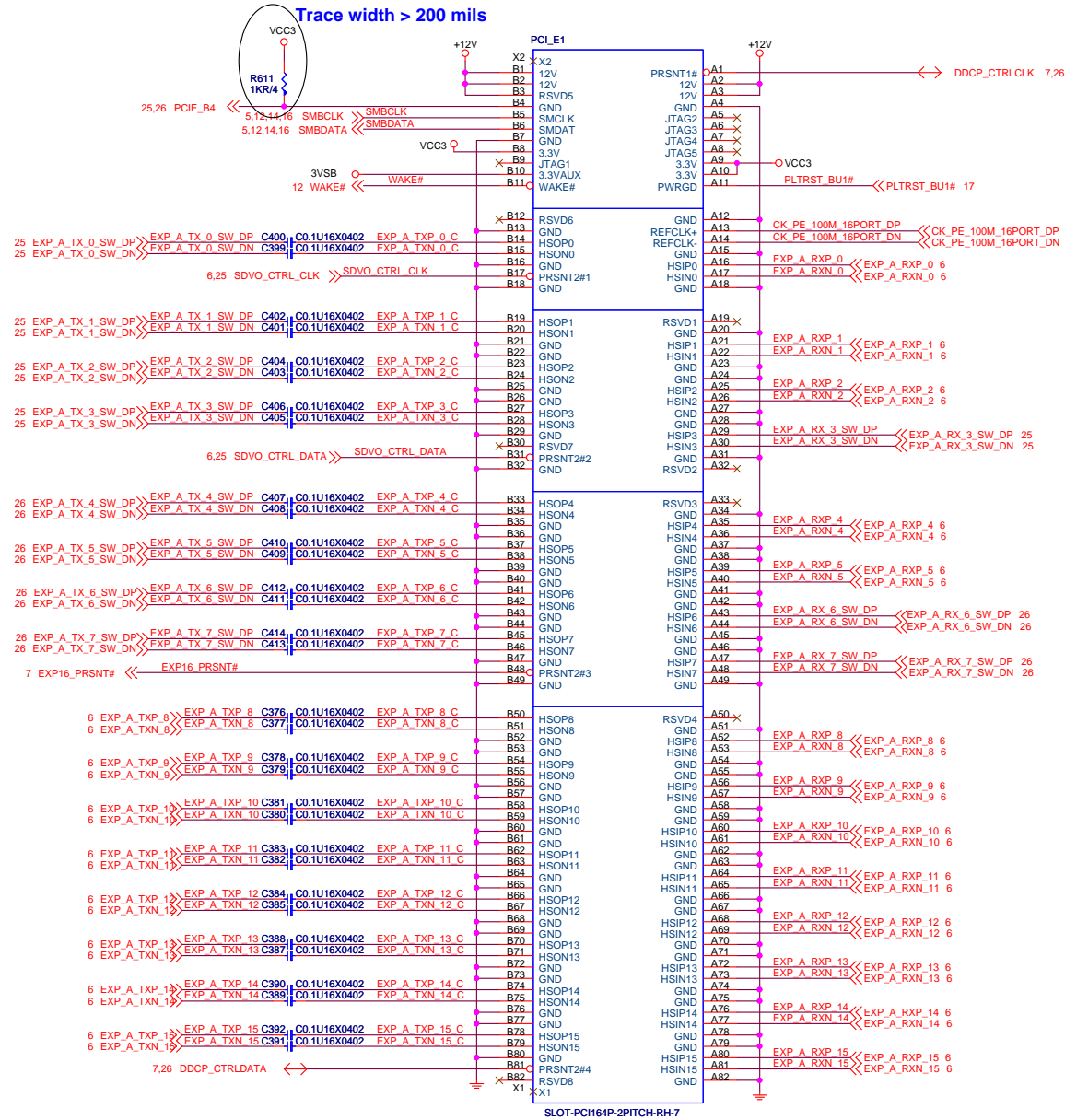
A1117 CO-LAY SOT223 (TO_261) PNP BJT



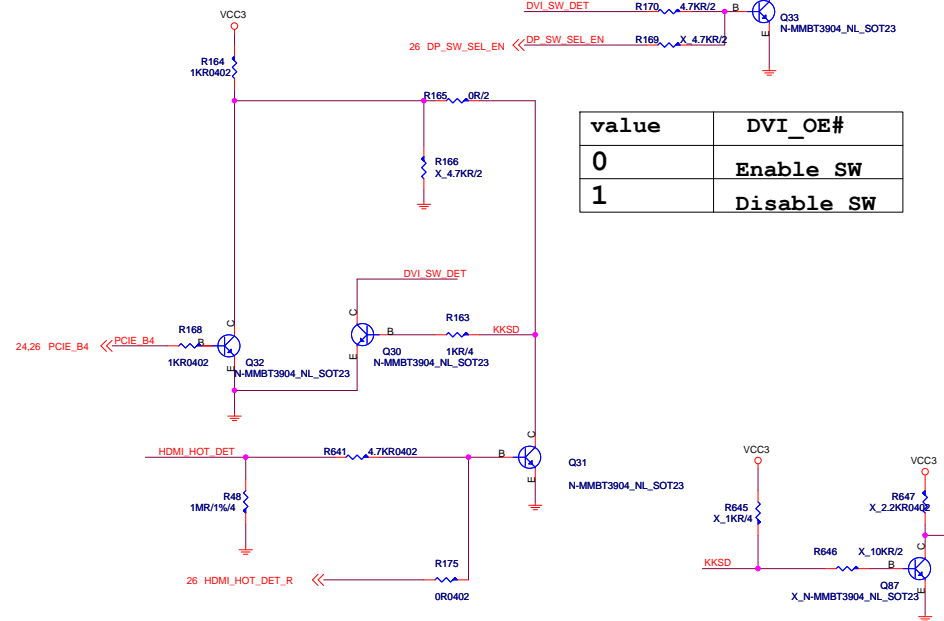


PCI Express X16 Slot

PCI Express X1 Slot

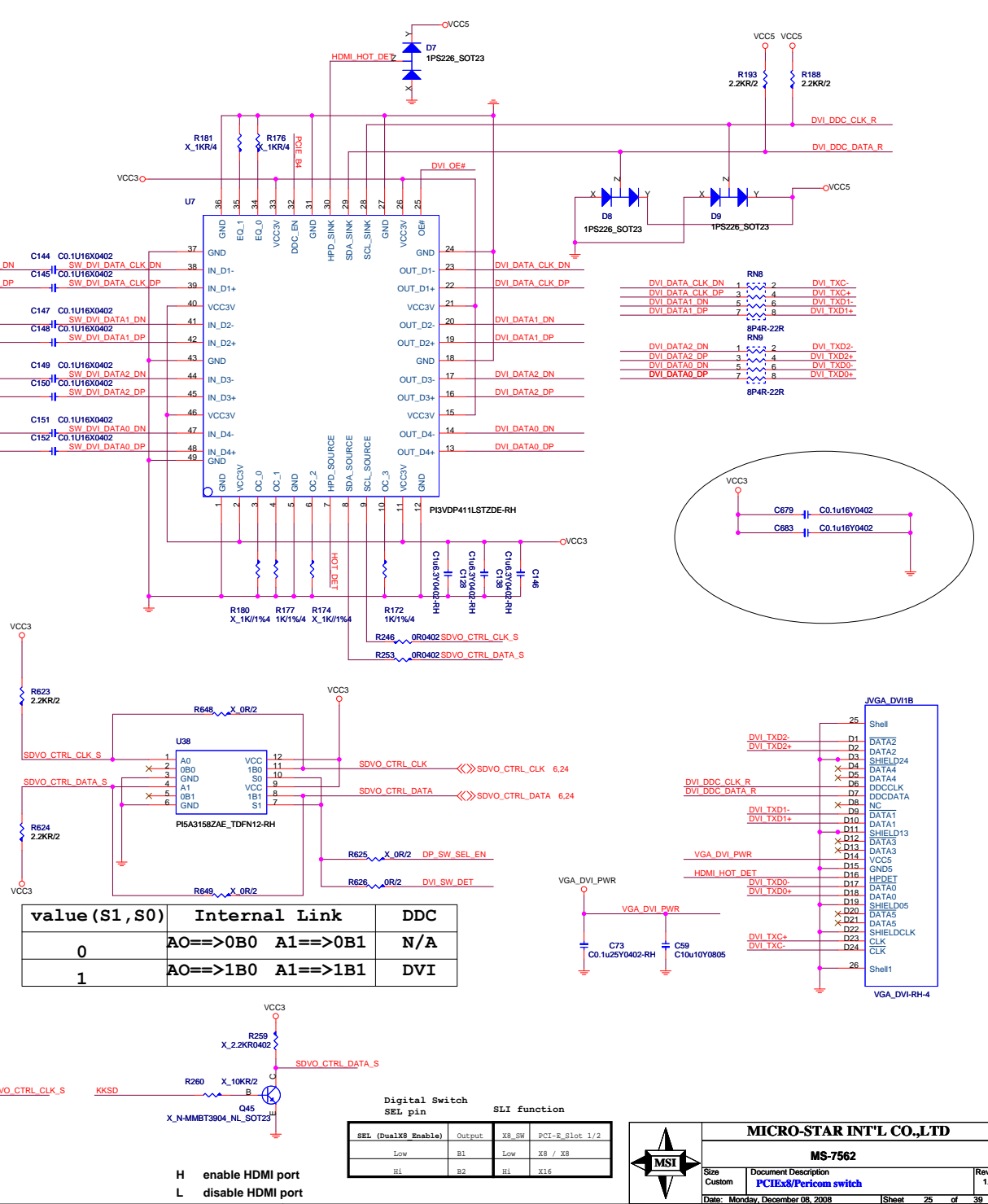


(Share PCI_E x4 form PCI_E x16 Slots)



value	DVI_OE#
0	Enable SW
1	Disable SW

value(S1,S0)	Internal Link	DDC
0	AO==>0B0 A1==>0B1	N/A
1	AO==>1B0 A1==>1B1	DVI



Digital Switch SEL pin		SLI function	
SEL (DualX8 Enable)	Output	X8_SW	PCI-E Slot 1/2
Low	B1	Low	X8 / X8
Hi	B2	Hi	X16

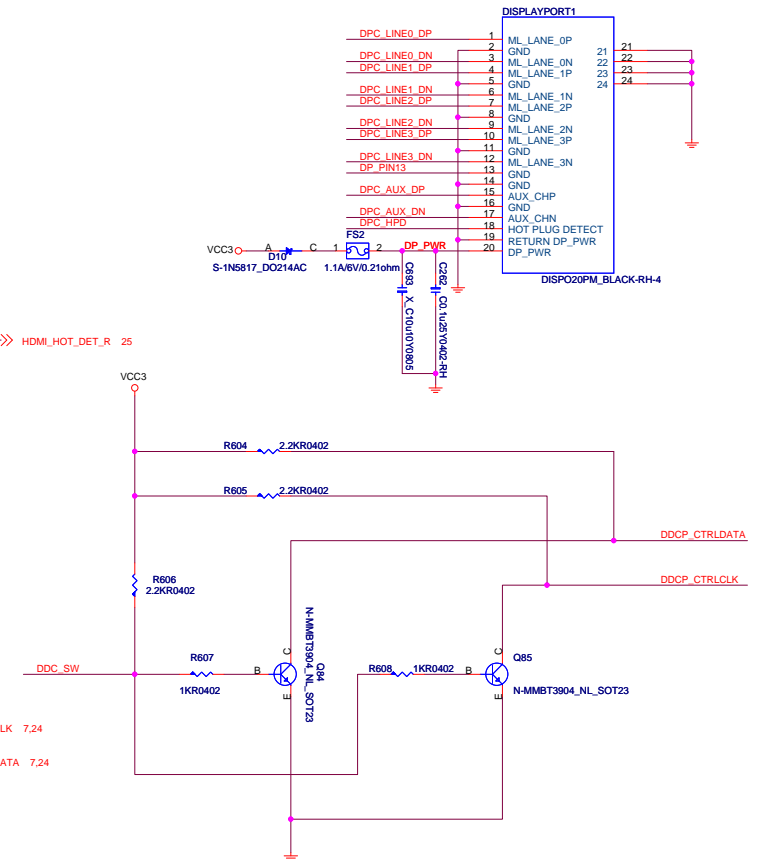
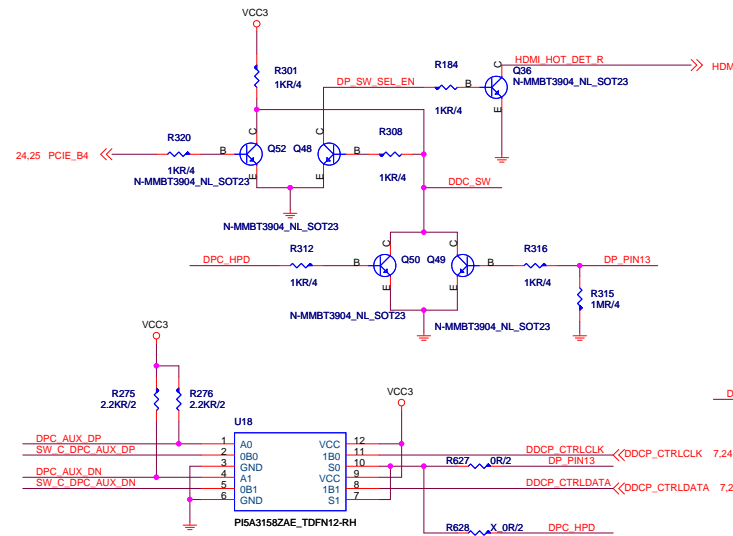
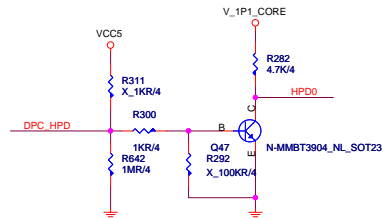


MICRO-STAR INT'L CO.,LTD

MS-7562

Size Custom	Document Description PCIEx8/Pericom switch	Rev 1.1
Date: Monday, December 08, 2008		Sheet 25 of 39

(Share PCI_E x4 form PCI_E x16 Slots)



value (S1,S0)	Internal Link	DDC
0	AO==>0B0 A1==>0B1	N/A
1	AO==>1B0 A1==>1B1	DP

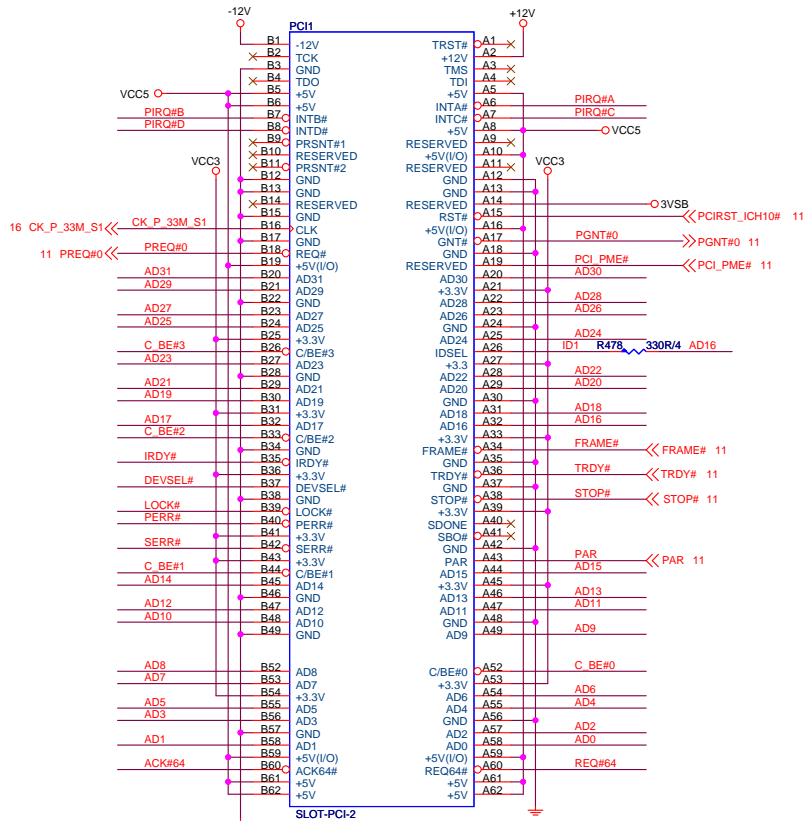


MICRO-STAR INT'L CO.,LTD

MS-7562

Size Custom	Document Description PCIEx8/Pericom switch	Rev 1.1
Date: Friday, December 05, 2008		Sheet 26 of 39

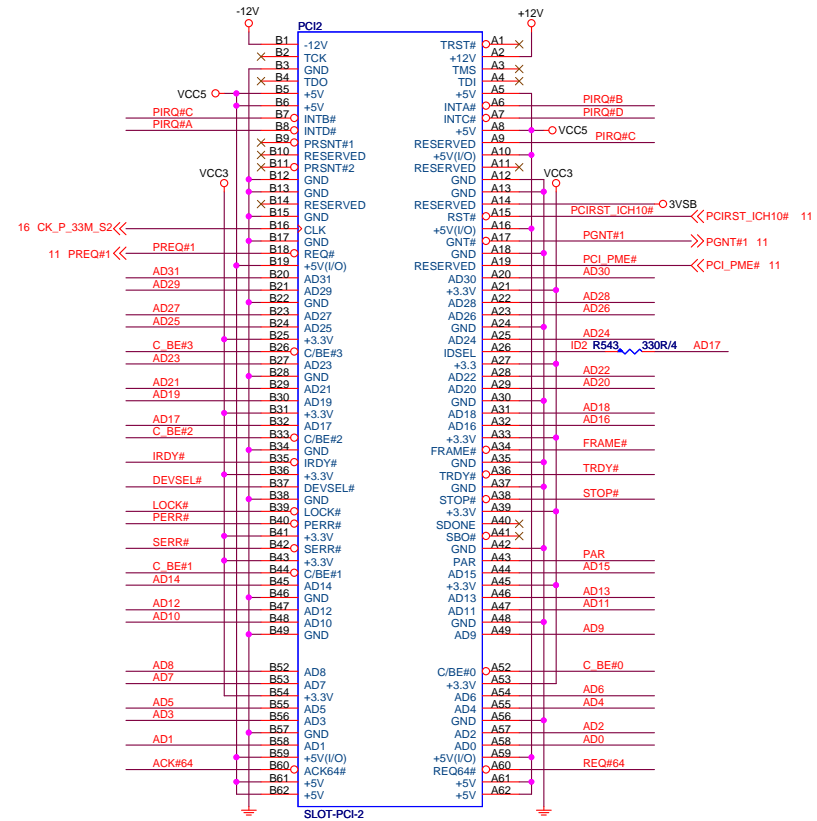
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



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PIRQ#A

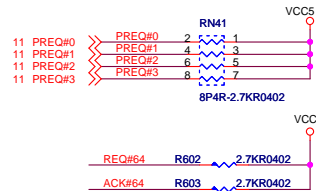
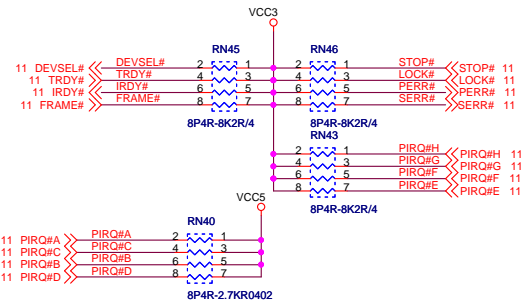
11 AD[31..0] << AD[31..0]
11 C_BE#[3..0] << C_BE#[3..0]

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

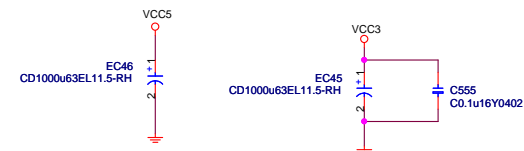


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

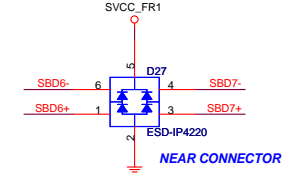
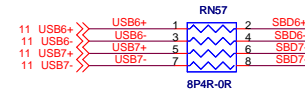
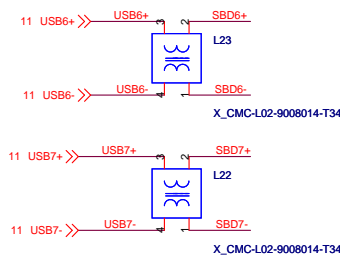
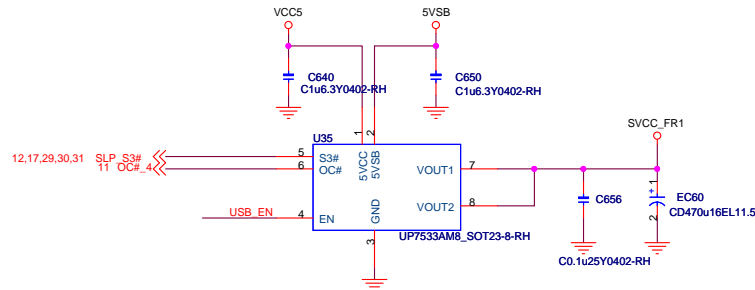


MICRO-STAR INT'L CO.,LTD

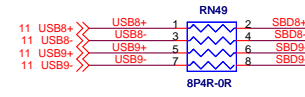
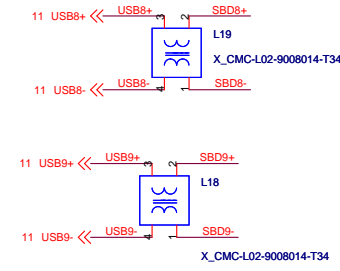
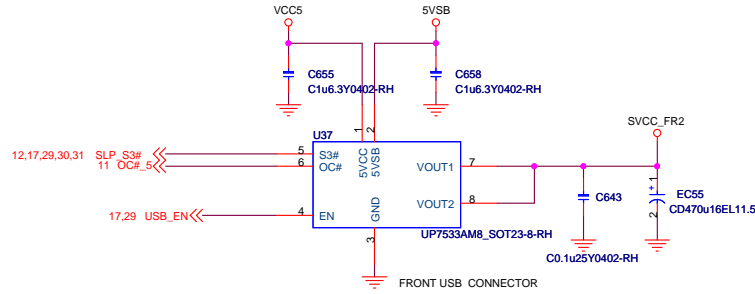
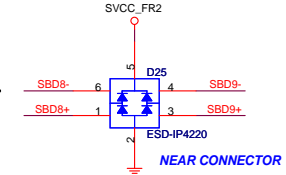
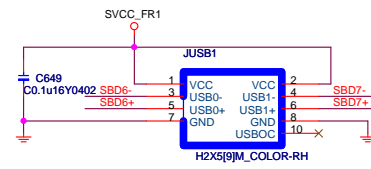
MS-7562

Size	Document Description	Rev
Custom	PCI Slot 1 & 2	1.1
Date: Monday, December 08, 2008	Sheet 27 of 39	

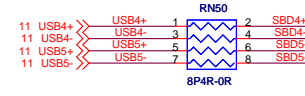
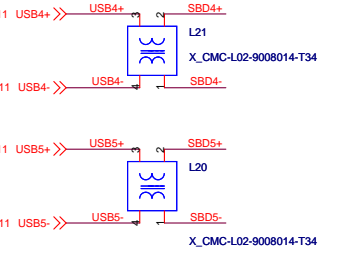
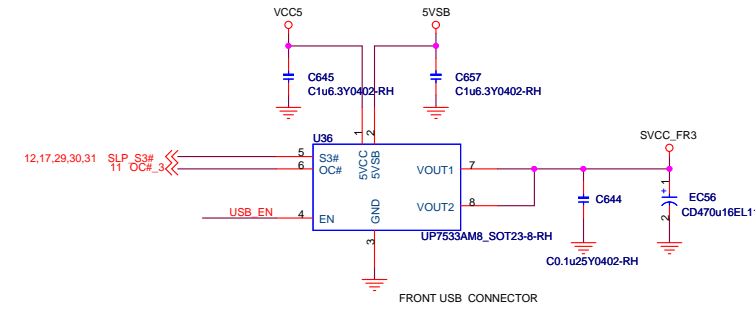
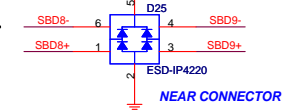
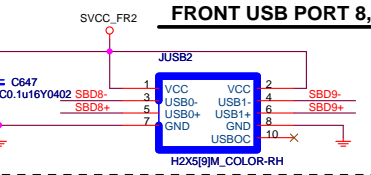
Front USB Connector



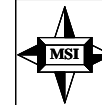
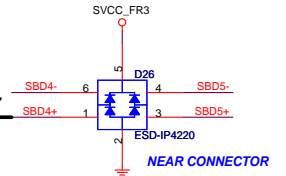
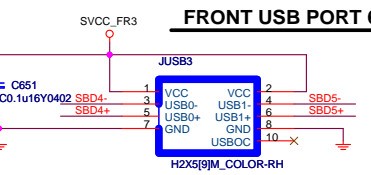
FRONT USB PORT2,3



FRONT USB PORT 8,9

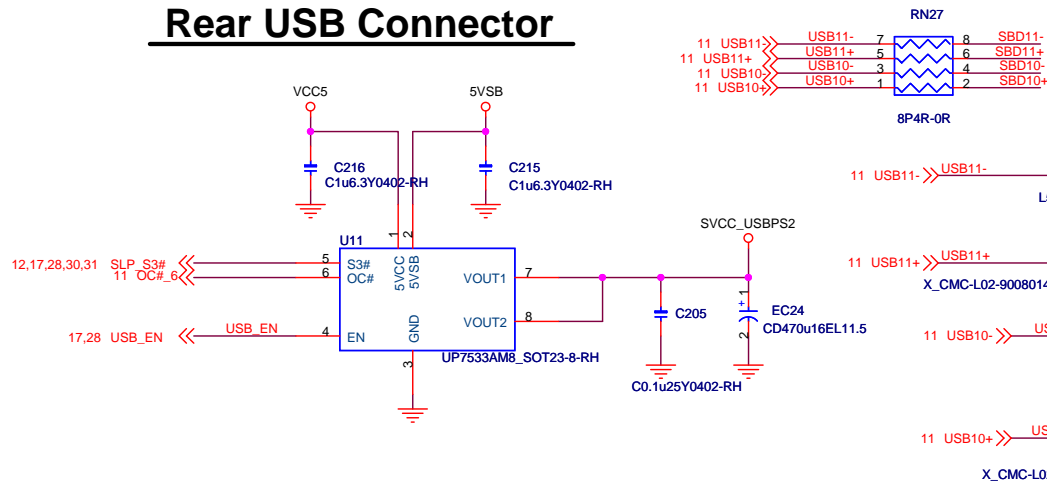


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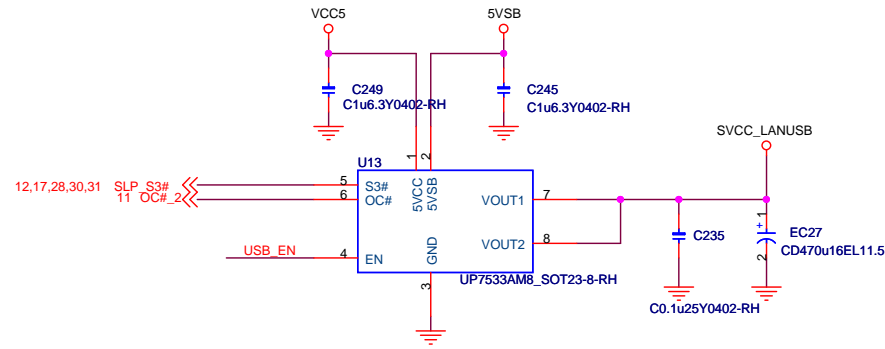
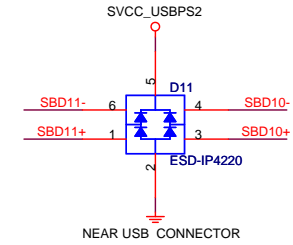
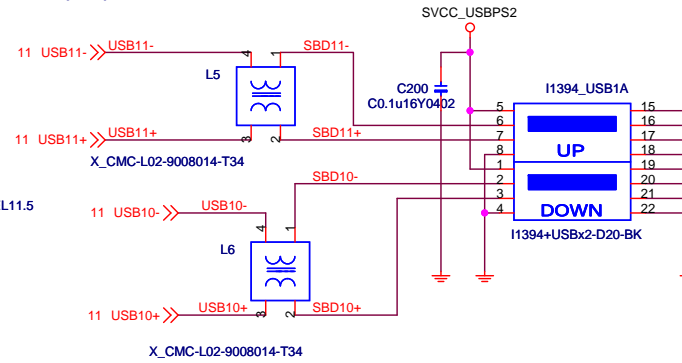


MICRO-STAR INT'L CO.,LTD			
MS-7562			
Size	Document Description		Rev
Custom	USB Connector		1.1
Date: Wednesday, December 03, 2008		Sheet 28 of 39	

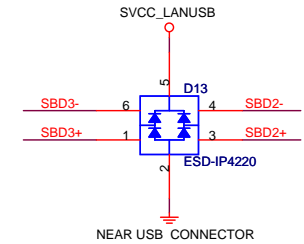
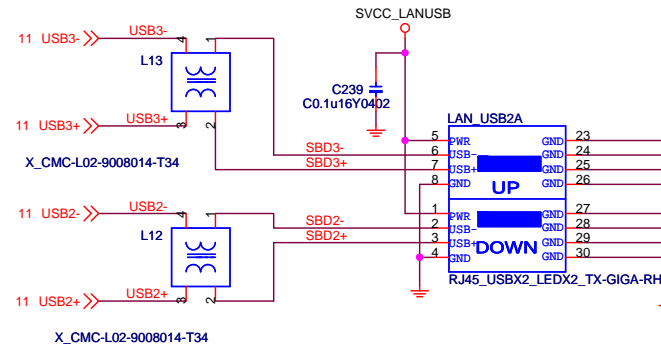
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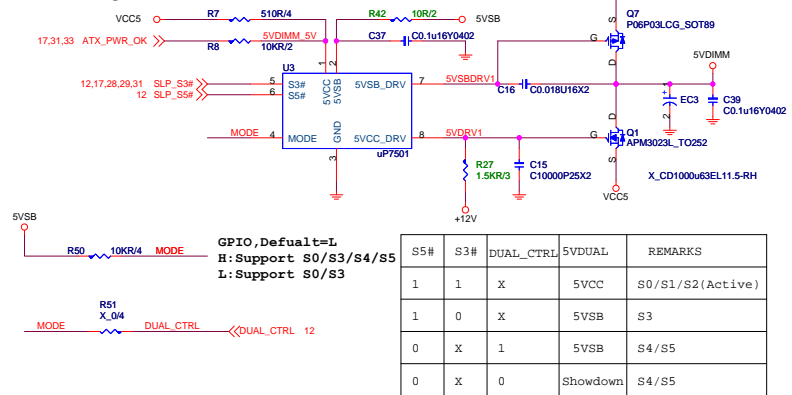
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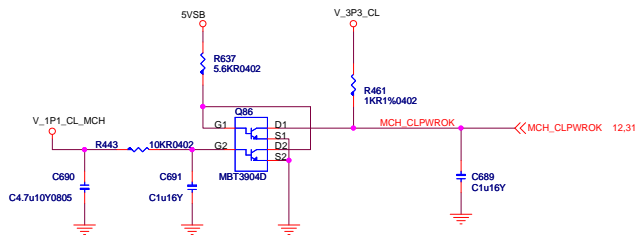
REAR USB PORT 0,1 (With LAN)



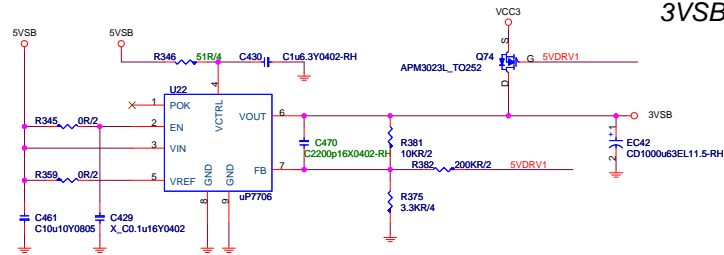
5VDIMM FOR DDR



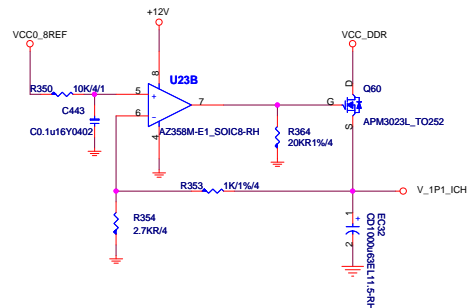
CL_PWROK



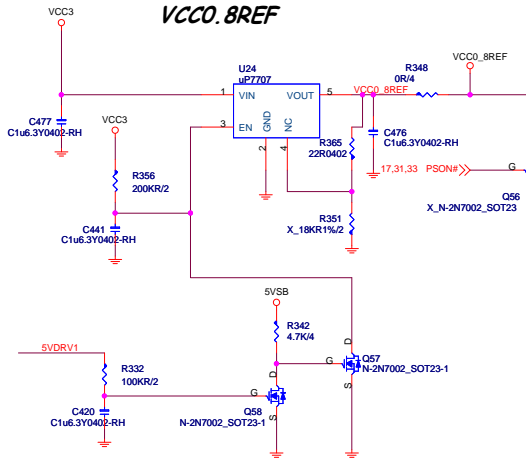
3VSB



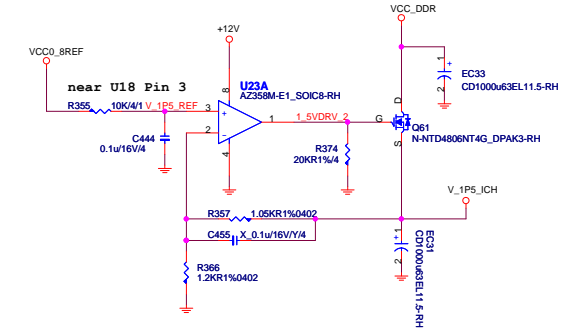
SB 1.1V 1.16A



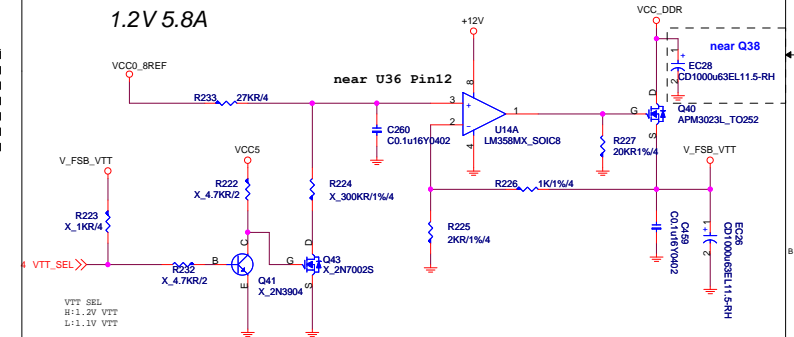
VCC0_8REF



SB 1.5V 2.4A

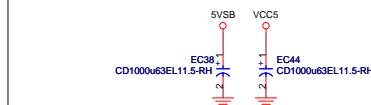


1.2V 5.8A



For power 700W solution
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

	S0	S3	S4	S5
DUAL_CTRL	X	X	0 1 1	0 1 1
5VSBDRV1	1	0	1 0 0	1 0 0
5VDRV1	1	0	0 0 0	0 0 0
5VSBDRV2	X	0	1 0 0	1 0 0
USB_MODE	X	1	X 1 0	X 1 0
5VDIMM	Y	Y	N Y Y	N Y Y
USB power	Y	Y	N Y N	N Y N

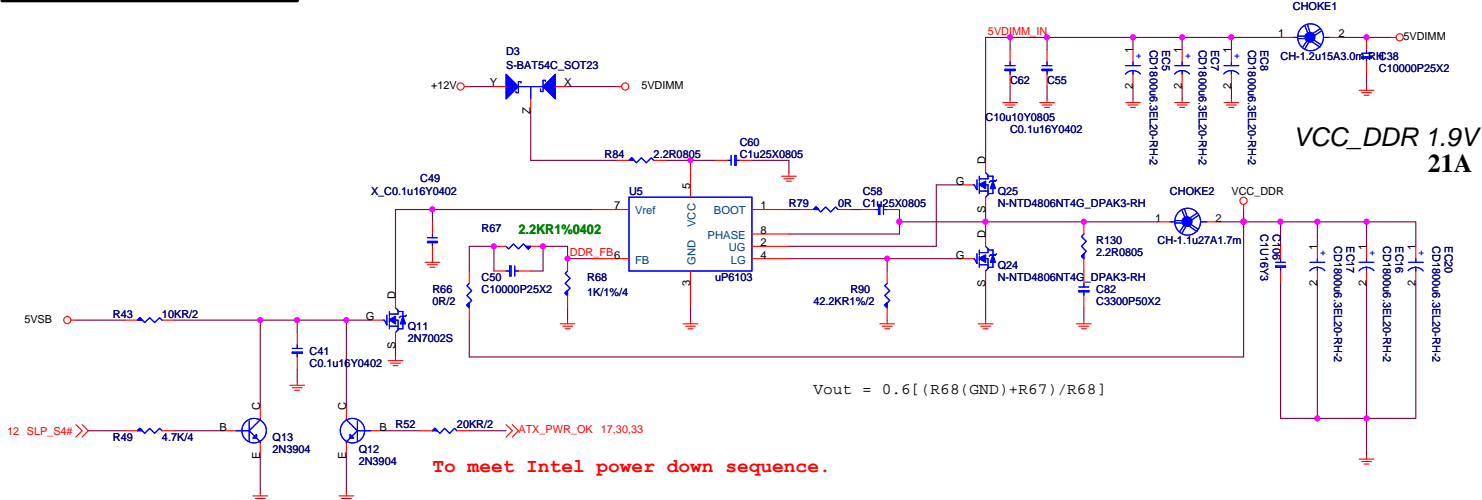


FIELD	OEM/ODM	CHANNEL
ADD	R26, R16, R30, R40, Q5	R6, R31
REMOVE	R6, R31	R26, R16, R30, R40, Q5
CHANGE	R5 => C5=0.1uF	C5=> R5=51Kohm

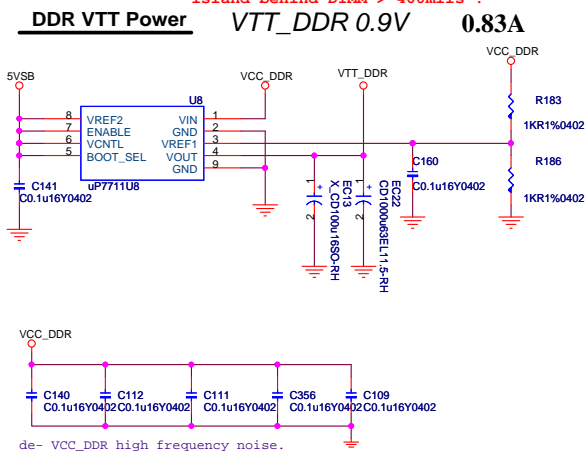


MICRO-STAR INT'L CO.,LTD			
MS-7562			
Size	Document Description	Rev	
Custom	ACPI controller UPI	1.1	
Date: Monday, December 08, 2008		Sheet 30 of 39	

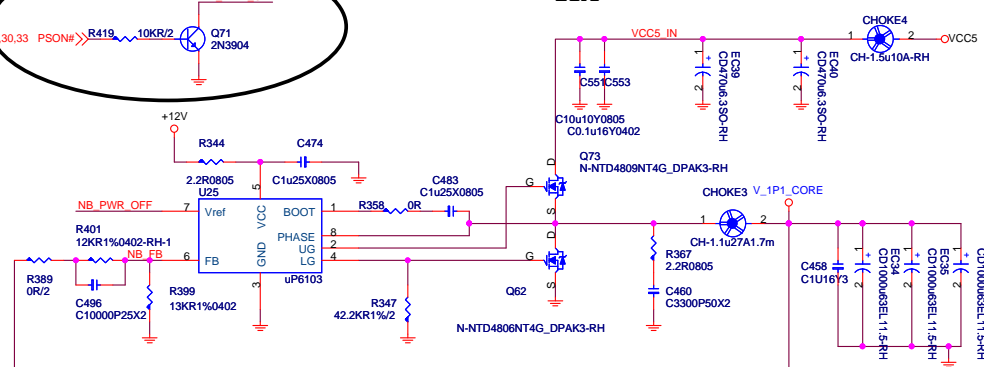
DDR II 1.9V POWER



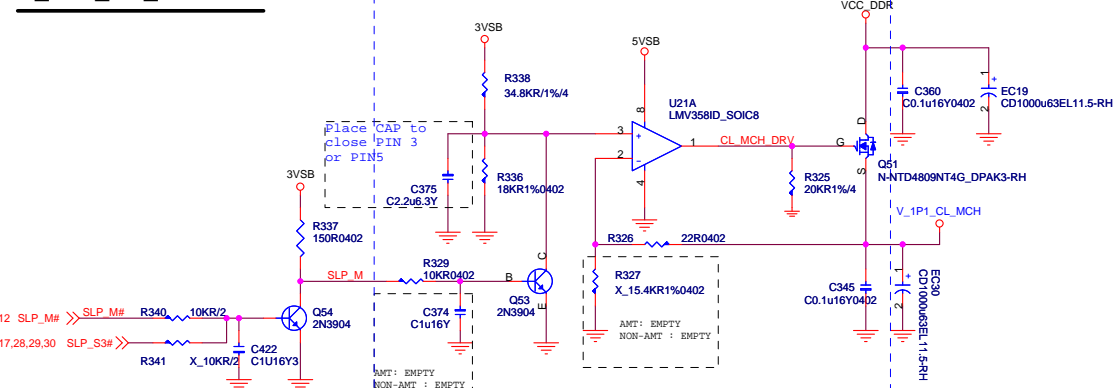
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



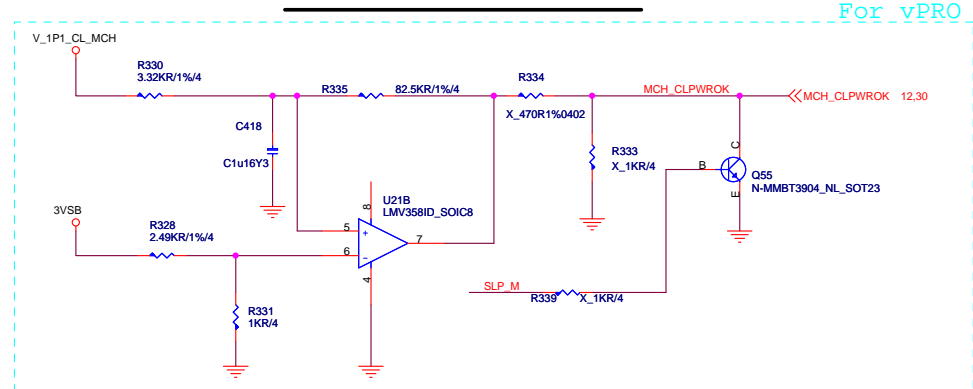
NB 1.1V POWER 21A



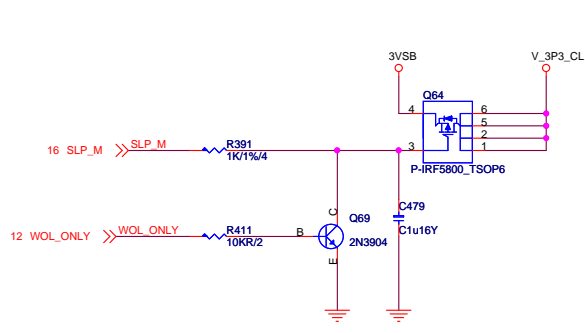
AMT POWER V_1P1_CL_MCH 3A



CLINK PWROK GENERATION For vPRO

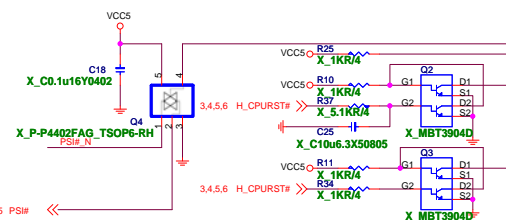
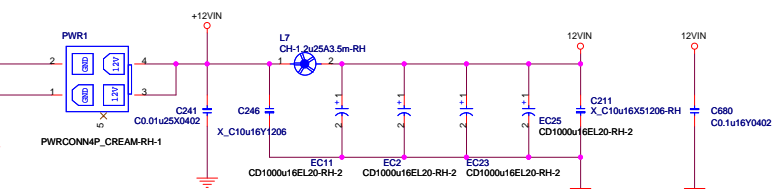
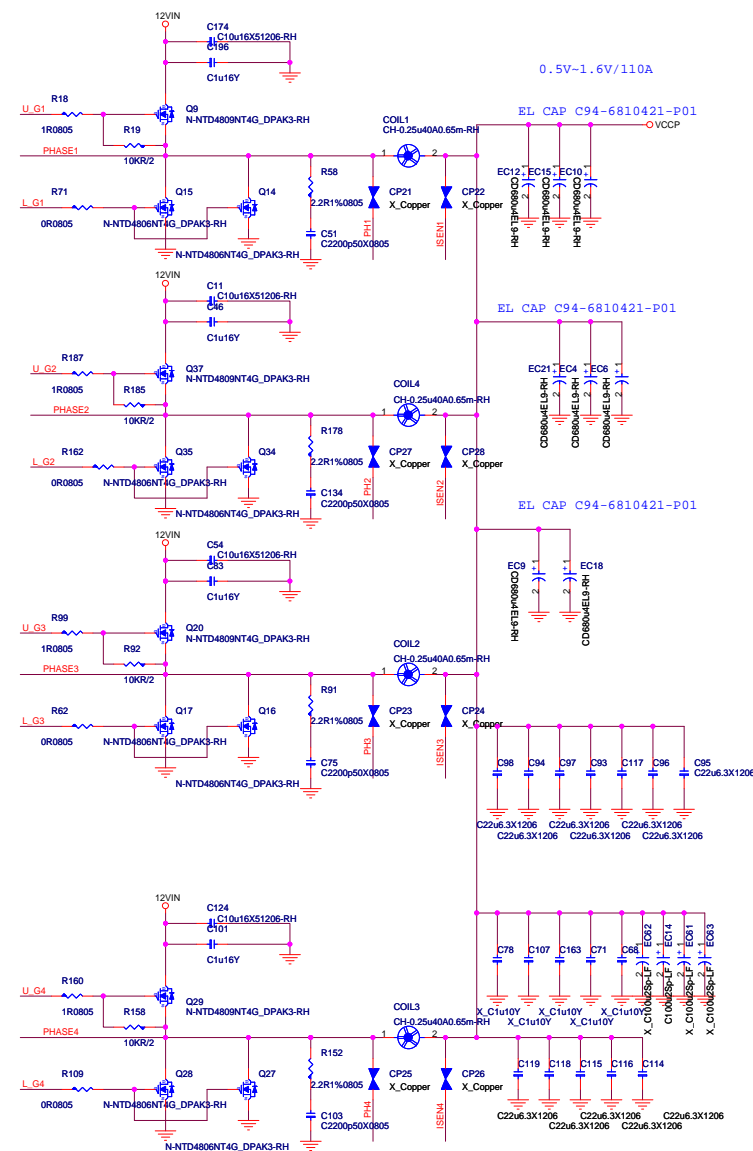
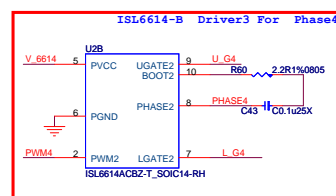
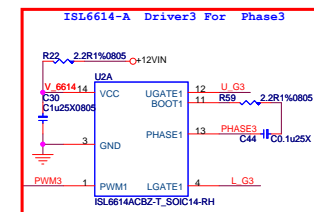
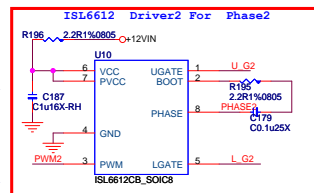
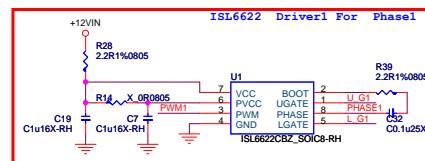
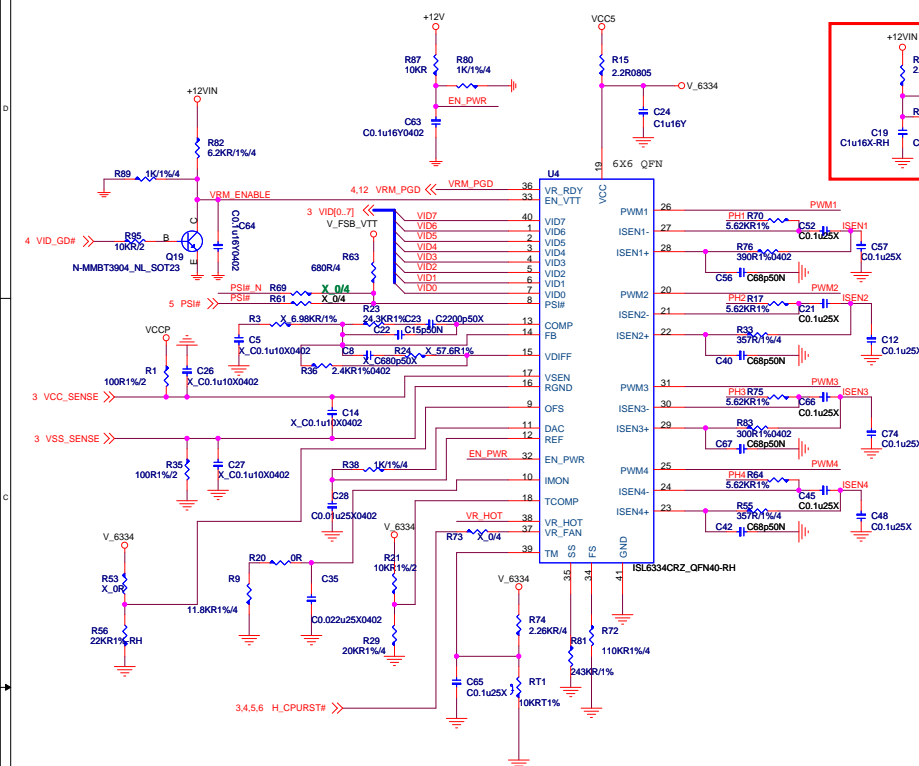


V_3P3_CL 711mA For vPRO



MICRO-STAR INT'L CO.,LTD			
MS-7562			
Size	Document Description	Rev	
Custom	NB Core Power & DDR Power	1.1	
Date: Wednesday, December 10, 2008		Sheet	31 of 39

ISL6334 4Phase



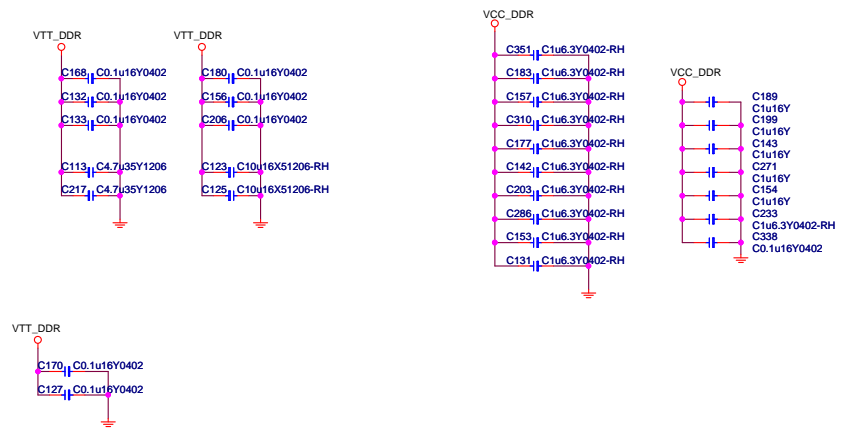
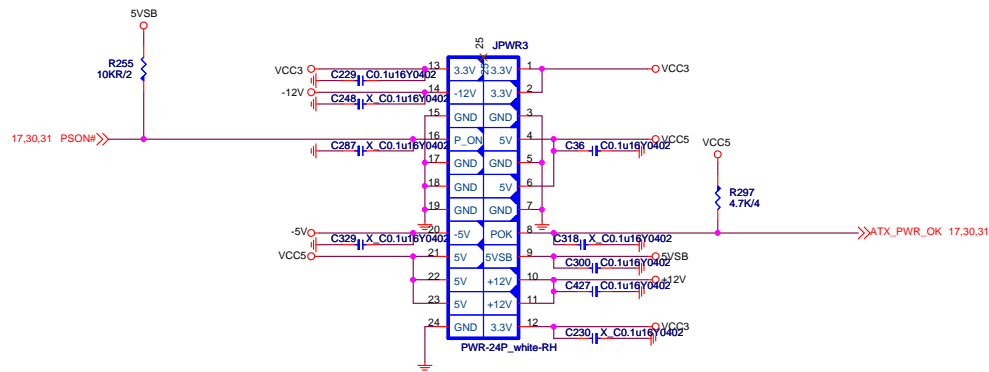
PDG:page 438 ,Please put near PWM



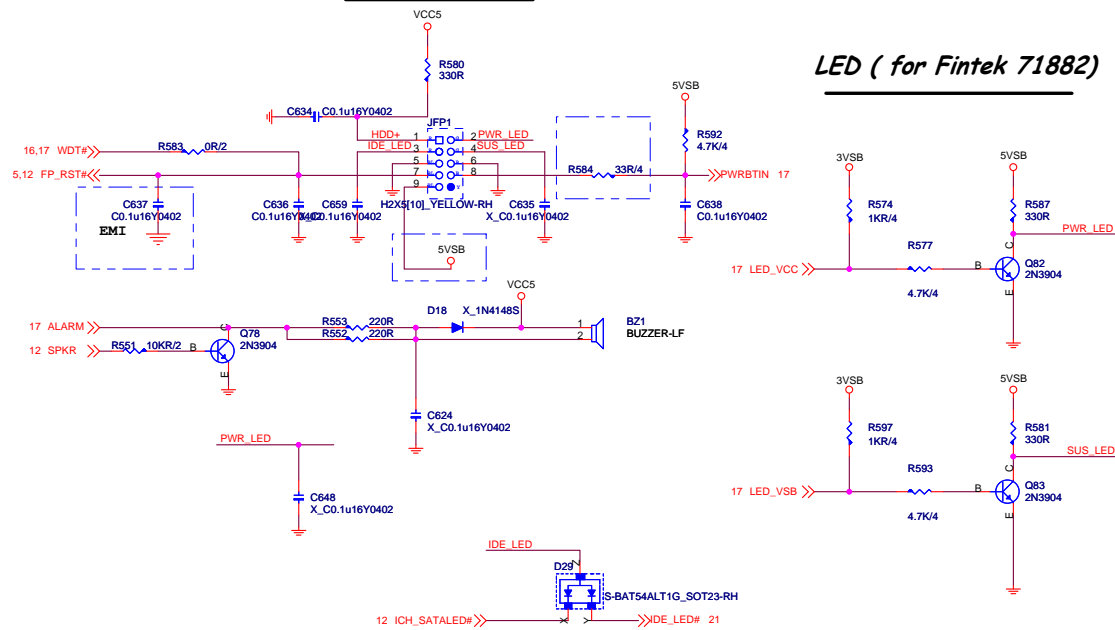
MICRO-STAR INT'L CO.,LTD

Size C	Document Description ISL6334 4-Phase Modulize circuit	Rev 1.1
Date: Wednesday, December 10, 2008	Sheet 32 of 30	

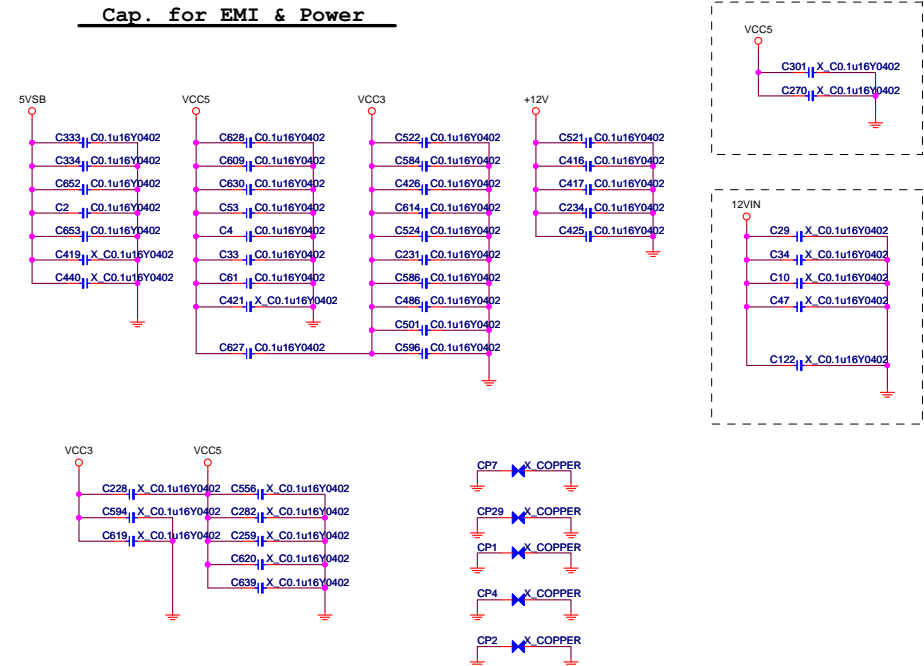
ATX POWER CONNECTOR



FRONT PANNEL



Cap. for EMI & Power



MICRO-STAR INT'L CO.,LTD

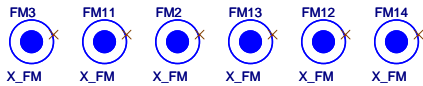
MS-7562

Size	Document Description
Custom	ATX PWR-Connector & Front Panel

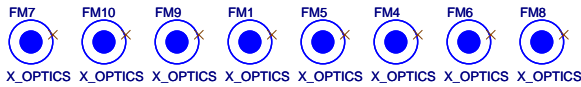
Rev	
1.1	

Date: Wednesday, December 03, 2008	Sheet 33 of 39
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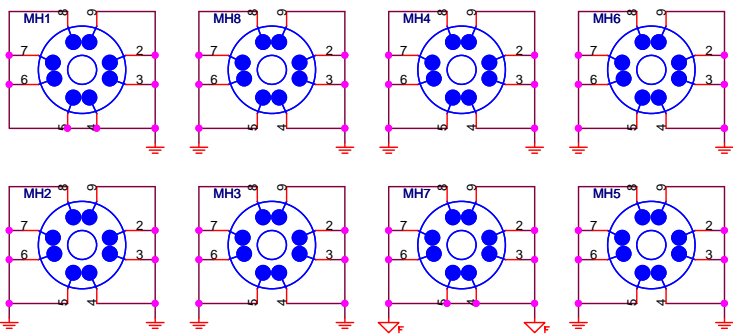
Optical Fiducial Marks-120



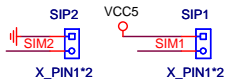
Optical Fiducial Marks-100



Mounting Holes



Simulation



JFP2(4-6)

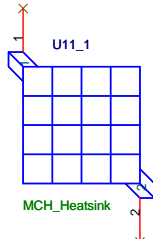
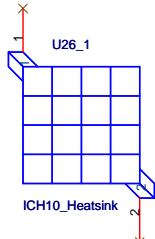


X_JUMPER-1X2A_green

BAT1_X



BATTERY-CR2032



MICRO-STAR INT'L CO.,LTD

MS-7562

Size B	Document Description Manual Parts & Option Parts	Rev 1.1
Date: Monday, December 08, 2008	Sheet 34 of 39	

Ver.	Change List	Page
0B	<p>1. VRM Modify</p> <p>Change R12,16,26,32 =>6.98Kohm ,C16 =>15pF R22=>300ohm,R39=>2.49Kohm,R43=>20Kohm Stuff EC3 EC9</p> <p>2. Power team recommend</p> <p>change C79=>10nF, EC31=>1000uF replace Q32,34=>D03-0480600-O05</p> <p>change C328=>10nF,EC33,34 =>remove,EC37,39=>470uF,EC32,35,36=>820uF ADD EC110 =>820uF replace Q43=>D03-0903BDB-N03,Q42,73=>D03-75N022B-N03</p> <p>3. Add Q72,R362 NB power switch circuit turn off NB power</p> <p>4. follow demo circuit Add R870 Stuff for NON-Intel LAN</p> <p>5. For DVI stuff R717,R718,R719, change RN79,RN80 => 22R</p> <p>6. R133=>1.58K,R295=>10.7K for DDR, NB power margin</p> <p>7. For customer requests change R909,R910=> 0603</p> <p>8. Change R92=> 1k for chip_power_good level</p> <p>9. Improve V_1P5_ICH VR's MOS temperature</p> <p>remove R326,C383,R320,R608,C379,EC100.R374,Q47 stuff EC41 replace Q52 => D03-75N022B-N03 ,U18=> I71-LM35833-B28</p> <p>10. VRM Modify Improve temperature</p> <p>replace Q2,Q3,Q7,Q9,Q10,Q14,Q15,Q17=> D03-75N022B-N03</p> <p>11. Add EC33 for V_FSB_VTT</p> <p>12. For INTEL Design Review</p> <p>Change C740 =>0.1u</p> <p>Add C980,C981,C982,C983 =>0.1u for VREF_CA_A,VREF_CA_B,VREF_DQ_A,VREF_DQ_B</p> <p>Near SB ball U1 Add C984,C985 =>0.022u</p> <p>Near SB ball AC9 Add C986 =>0.1u</p> <p>For VccGLAN1_5 change C445=>4.7u/X5R ,C443=>2.2u/X5R</p> <p>For 5VREF ,5VREF_SUS change C571 ,C611=>1uF/X7R</p> <p>For VccRTC near the ball A22 C505 => 1uF/Y5V</p> <p>For V_1P05_VCCAUX Add C987=>0.1uF/X7R ,C561 => 1uF/Y5V</p> <p>For VCCA_EXP</p> <p>remove L29 , Add R915=>1Ω ,L39 = 600 Ω (FB) ,C612=> 1uF</p> <p>For VCCA_DAC</p> <p>Add L39 = 600 Ω (FB) , change R892 =>1Ω ,</p> <p>For VCCDQ_CRT</p> <p>Add L40 = 600 Ω (FB) , change R702 =>1Ω ,C613=>1u C613 will be 1u for onbroad graphic BOM Option will be 0 ohm for no onbroad graphic</p> <p>For FSB_VTT require</p> <p>Add C988 C989 C990=> 2.2uF</p> <p>For VCC_Core require backside caps 10uF x(3/4) and 1uF x(6/8)</p> <p>C300,C562,C767=> 10uF change C307 C323 C382 C416 C884 C975 C977 C371 =>1u</p> <p>VCC_Core require caps 22uF x3, 1uF x3 and 10uF x3</p> <p>Add C991,C992.C993 => 22uF Add C763 C765 C762 =>10uF change C976 C302 C311 =>1uF</p> <p>VCC_EXP require caps 2.2uF x3</p> <p>Add C994,C995.C996 => 22uF</p> <p>VCCSM require caps 2.2uF x6</p> <p>change C262=2.2uF , ,Add C263,C264,C269,C268,C267 =>2.2uF</p>	<p>30</p> <p>29</p> <p>29</p> <p>12</p> <p>24</p> <p>29</p> <p>13</p> <p>28</p> <p>28</p> <p>30</p> <p>28</p> <p>08</p> <p>14,15</p> <p>13</p> <p>13</p> <p>13</p> <p>13</p> <p>13</p> <p>09</p> <p>09</p> <p>09</p> <p>09</p> <p>09</p> <p>09</p> <p>09</p> <p>09</p> <p>09</p> <p>09</p>

Ver.	Change List	Page
0B	<p>For SRTCST# Required</p> <p>change R456 => 20KΩ and C513=>1uF</p> <p>For NB1.AR2 Required</p> <p>change R706 Empty R709 stuff</p> <p>13. Reserve R578 Q47 R478 & Add R802 for Plug - in issue</p> <p>14. For INTEL Design Review change C262 to 2.2uF Add C250</p> <p>15. Change VGA DVI to new VGA DVI (N58-39F0031-SK7)</p> <p>16. COM1 change to JCOM1</p> <p>17. Add R872 & R873 for NB&DDR power layout</p> <p>18. Add U56,C997,C998,C999 ,EC108 for KB/MS power circuit</p> <p>19. change SVCC1,SVCC2 to SVCC_Real</p> <p>change SVCC3,SVCC4 ,SVCC4 to SVCC_Front</p> <p>change SVCC6 to SVCC_MCR</p> <p>SWAP JUSBF & JUSBMRC</p> <p>20. ADD C674,C675C677,C680 For EMI</p> <p>21. change R780,R778,R777,R776 for audio Precision</p> <p>22. Reserve for Plug - in issue SWAP Q47 D,S</p> <p>23 Change Vaule Empty or Stuff state In Shm circuit For P45 + ICH10 SKU</p> <p>24 follow intel demo Design change R227 to 150R</p> <p>25 No-stuff R514, Stuff R505 with 10Kohm</p>	<p>12</p> <p>09</p> <p>30</p> <p>09</p> <p>18,24</p> <p>17</p> <p>29</p> <p>17</p> <p>26</p> <p>27</p> <p>27</p> <p>31</p> <p>22</p> <p>30</p> <p>29</p> <p>12</p>

- Disable PSI# patch circuit.
Empty (-)R242,R253,R273,R247,C235,Q53 ,Q65 Stuff R652
- DDR3 Power Correction.
Change R133 1.58K1% to 1.5K1%
- Beep sound
Empty R75
- Replace USB connector.
N53-08M0171-K06 ==> N53-08M0191-F02
- Remove HDA Function.
Empty (-)R860,R861,R862,R863,R864,R865,R866,R867,R859 ,JHDA1
- LAN USB connector
Empty
- SIO related Issues.
Empty (-)R789 (+)R112



MICRO-STAR INT'L CO.,LTD		
MS-7562		
Size Custom	Document Description Revision History	Rev 1.1
Date: Wednesday, December 03, 2008 Sheet 35 of 39		